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Non-volatile Memory Devices beyond Process-scaled Planar Flash Technology

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Non-volatile Memory Devices beyond Process-scaled Planar Flash Technology

by

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Dedication

To my parents Bharati and Tapan Kumar Sarkar, whose selfless and limitless love, hardships, sacrifices and support have carried me through each step of my way through life.

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Non-volatile Memory Devices Beyond Process-scaled Planar Flash Technology

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Supervisors: Sanjay K. Banerjee and Robert J. Gleixner

Mainstream non-volatile memory technology dominated by the planar Flash transistor with continuous floating-gate has been historically improved in density and performance primarily by means of process scaling, but is currently faced with significant hindrances to its future scaling due to fundamental constraints of electrostatics and reliability. This dissertation is based on exploring two pathways for circumventing scaling limitations of the state-of-the-art Flash memory technology. The first part of the dissertation is based on demonstrating a vertical Flash memory transistor with nanocrystal floating-gate, while the second part is based on developing fundamental understanding of the operation of Phase Change Memory.

A vertical Flash transistor can allow the theoretical minimum cell area and a nanocrystal floating-gate on the sidewalls is shown to allow a thinner gate-stack further conducive to scaling while still providing good reliability. Subsequently, the application of a technique of protein-mediated assembly of preformed nanocrystals to the sidewalls of the vertical Flash transistor is also demonstrated and characterized. This technique of

ordering pre-formed nanocrystals is beneficial towards achieving reproducible nanocrystal size uniformity and ordering especially in a highly scaled vertical Flash cell, rendering it more amenable to scaling and manufacturability. In both forms, the vertical Flash memory cell is shown to have good electrical characteristics and reliability for the viability of this cell design and implementation.

In the remaining part of this dissertation, studies are undertaken towards developing fundamental understanding of the operational characteristics of Phase Change Memory (PCM) technology that is expected to replace floating-gate Flash technology based on its potential for scaling. First, a phenomenon of improving figures of merit of the PCM cell with operational cycles is electrically characterized. Based on the electrical characterization and published material characterization data, a physical model of an evolving "active region" of the cell is proposed to explain the improvement of the cell parameters with operational cycles. Then, basic understanding is developed on early and erratic retention failure in a statistically significant number of cells in a large array and, electrical characterization and physical modeling is used to explain the mechanism behind the early retention failure.

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CHAPTER 1

Introduction

The scientific, technological as well economic motivation behind the subject of this dissertation is explained and discussed in this chapter. The topic of this dissertation is placed in the context of evolution of non-volatile memory technology and relevant prior-art is discussed. Limitations of state-of-the-art planar Flash technology are described, and potential advancements offered by the proposed and demonstrated proof-of-concept devices with an alternative vertical cell design are discussed, the details of which constitute Part I of this dissertation. The remaining portion of this chapter discusses the background of Phase Change Memory, an alternate non-volatile memory technology with the potential for replacing mainstream floating-gate Flash technology, studies on which constitute Part II of this dissertation.

1.1 Motivation

Non-volatile memory is a pre-dominant semiconductor technology with widespread use in nearly all kinds of electronic devices. Simultaneously, non-volatile memory technology is witnessing an explosive growth with the wide proliferation and convergence of music players, smart cellular phones, digital cameras, digital assistants, hybrid and solid-state drives and other portable consumer electronic items. While every newer generation of these gadgets are placing increasing demands on the density and performance of the built-in Flash memory chips, conventional planar Flash memory

technology is widely regarded as being faced with fundamental physical limitations of process scaling that has contributed to its density and performance enhancements over the last couple of decades.[1] It therefore becomes necessary to explore alternative device designs and technologies which can offer a continued path for memory density and performance enhancements well into the future, thus ensuring progressively lower cost per bit, in turn enabling an even wider application space and growth of non-volatile memory technology. Thus, research work on two different approaches for circumventing the limitations of planar Flash memory technology constitutes the crux of this dissertation:

1. Design, fabrication and characterization of a vertical, three-dimensional Flash transistor/cell architecture with nanocrystal floating-gate for which the array density and reliability is limited by the available lithographic technology, rather than electrostatics.
2. Device physics, reliability and modeling studies on Phase Change Memory technology (pursued at Intel Corporation). Phase Change Memory has recently emerged as the most promising non-volatile memory technology to eventually succeed Flash memory and is expected to be scalable to 10 nm or perhaps even smaller dimensions, with expected improvements in some of its figures of merit with scaling.[2]

It is hoped that these twin approaches to circumventing the challenges to traditional Flash memory scaling would be complementary pathways in the quest for continued enhancement of the capabilities of non-volatile memory technology in the decades to come.

1.2 Background and review of challenges to conventional Flash memory technology

The planar Flash memory transistor was invented by Fujio Masuoka of Toshiba Corporation, reported in 1984[3] and first productized by Intel Corporation in 1988. It has since been aggressively scaled primarily through several process (lithographic) nodes to become the pre-dominant non-volatile memory technology with the fastest growth rate and more than $ 20 billion market (in 2005).[4] Keeping the basic overall memory transistor structure more or less the same, the scaling has so far been primarily achieved with lithography and various self-alignment schemes, hand-in-hand with the development of successive generations of the process technology that has made Moore's law a reality. Starting with the 256 kb array with 2.0 μm design rule proposed by Masuoka, state-of-the-art technology has progressed beyond 1 Gb and 4 Gb array capacities for NOR (Intel) and NAND (Samsung) Flash respectively, at the 65 nm technology node.[5] Figure 1.1 illustrates the historical trend of manufacturable cell-size and design rule scaling of NAND Flash, which is the driver for most aggressive scaling in the non-volatile memory technology space. The greater than 30x lithographic scaling and 40x and higher density scaling over past two decades of Flash technology has been accompanied by a precipitous drop in cost-per-bit: ~ 1000x over the last decade to ~ $ 25/Gb. The latter fact has been instrumental in enabling the proliferation and growth of solid-state non-volatile memory as a mainstream semiconductor product. The growth of the Flash memory application-base has in turn fueled the necessity and demand for continuing enhancements of the capacity, performance and cost-per-bit of Flash memory chips. However, the exponential enhancements in the capabilities of Flash memory technology have now led it to a critical juncture in its evolution. It is widely understood that the scaling trend historically possible largely with lithographic shrinking of the cell architecture is not sustainable

beyond the 45 nm technology node for NOR Flash and possibly 32 nm (or similar) for NAND Flash.[1, 6]

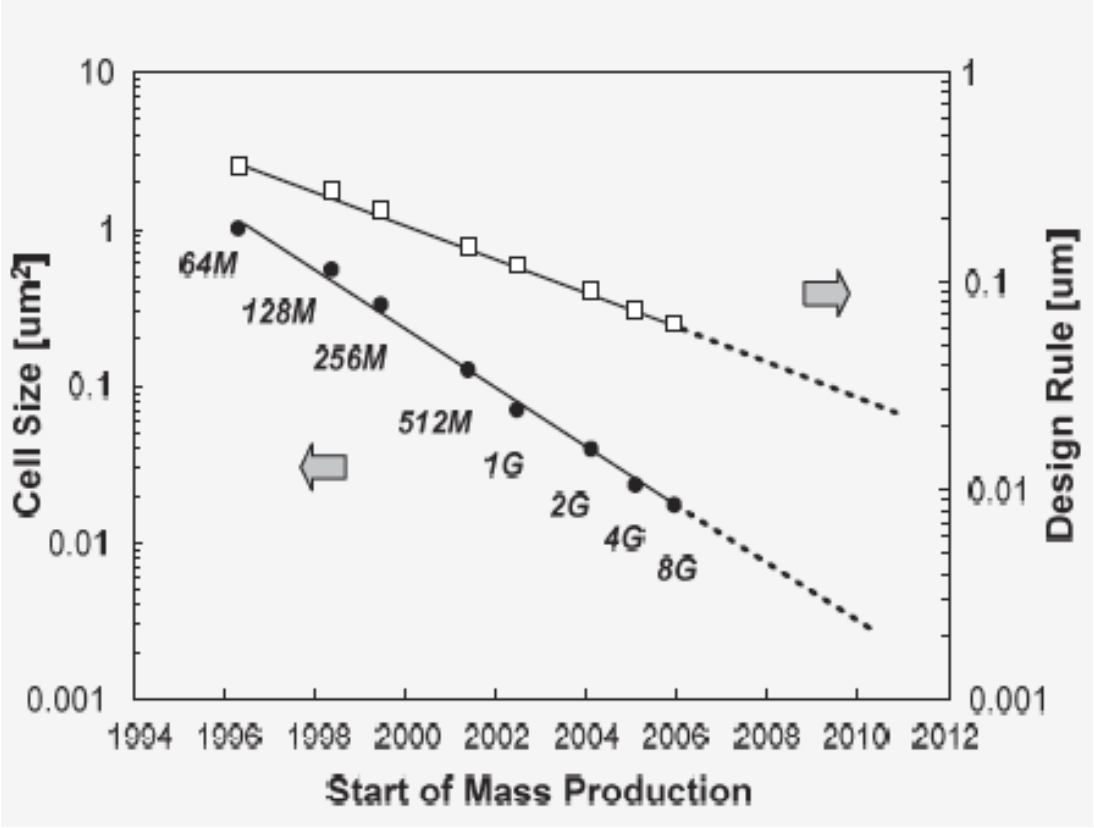
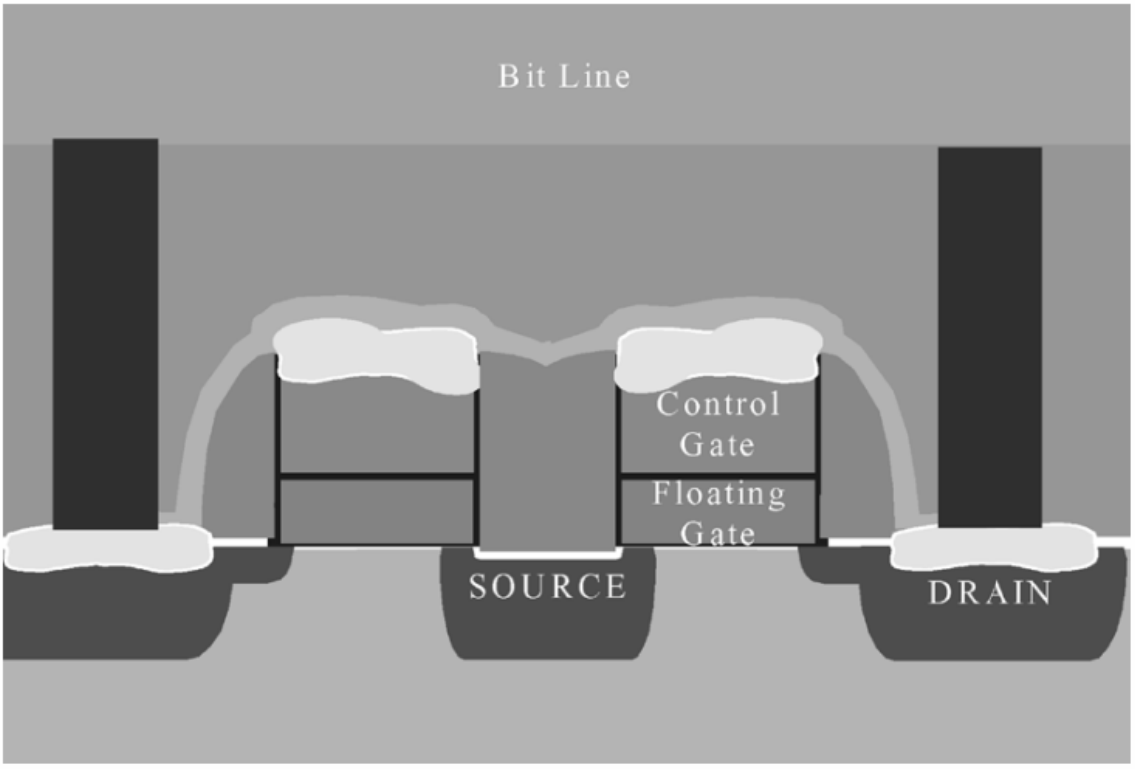


Figure 1.1: Historical trend and future prospects of NAND Flash memory densities and technology.[6]

Challenges to the scaling of conventional Flash memory technology in the sub-100 nm feature-size regime can be categorized by physical (lithographic), electrostatic (voltage) and reliability (leakage) related limits. The gate-length of a Flash transistor is primarily limited to $\geq$ 70 nm for supporting (i.e. preventing punch-through and Drain-Induced-Barrier-Lowering effects resulting from) about 4.5 V of potential difference between the transistor drain and source necessary for Hot Carrier Injection based programming. Similarly, the gate-width constrains the drive current necessary for fast

reading (access times) of the memory states. The high gate-voltages necessary during the memory program and erase operations also require a thicker gate-stack and isolation that in turn limits scaling of transistor physical dimensions. On the other hand, charge-leakage compromises the memory characteristics of a short-channel device designed with a thinner gate-stack for retaining adequate electrostatic coupling between the control-gate, floating-gate and channel.[7] In essence, the competing requirements of retention, endurance, performance and density, as illustrated in figs. 1.2 and 1.3, have been pushed nearly to their limits in a state-art-of-the-art Flash transistor. Hence, several generations of the industry-standard planar Flash transistor with a continuous polysilicon floating-gate have been limited to a minimum tunnel oxide thickness of 8 nm and correspondingly large channel dimensions for ensuring the 10-year data retention requirement.[8] Strict requirements on dielectric quality, device isolation and similar processing difficulties have also limited the scalability of the planar Flash transistor and array. These factors have threatened the enhancement of integration density and performance of Flash memory arrays by lithographic shrinking alone, requiring the exploration of fundamentally different approaches to Flash technology improvement. In the light of the above, the research work on an alternative cell design and an alternative technology described in this dissertation was pursued.



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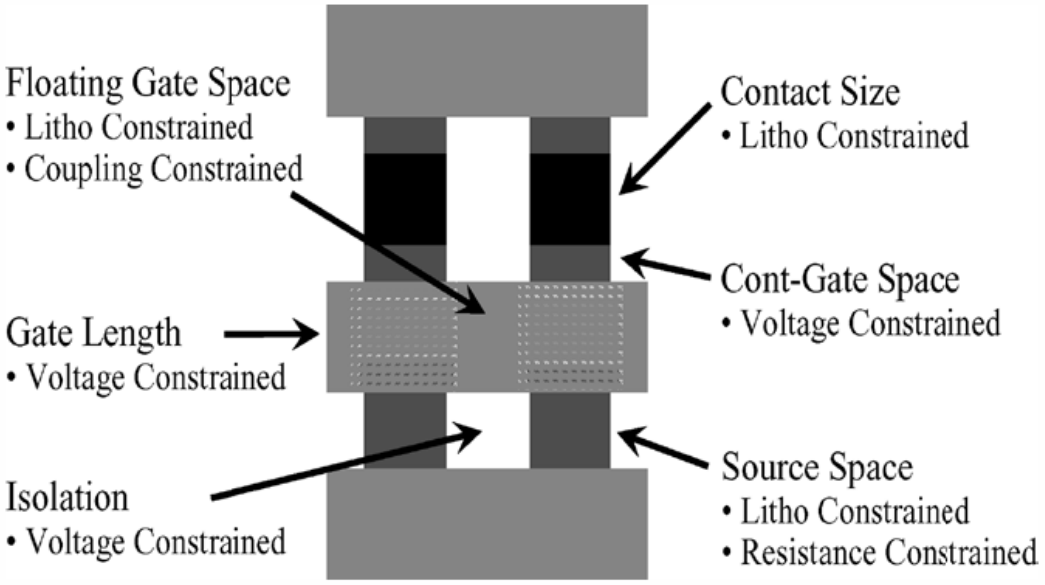


Figure 1.2: (a) Planar Flash cell cross-section along the channel, (b) Flash cell layout and major scaling constraints.[1]

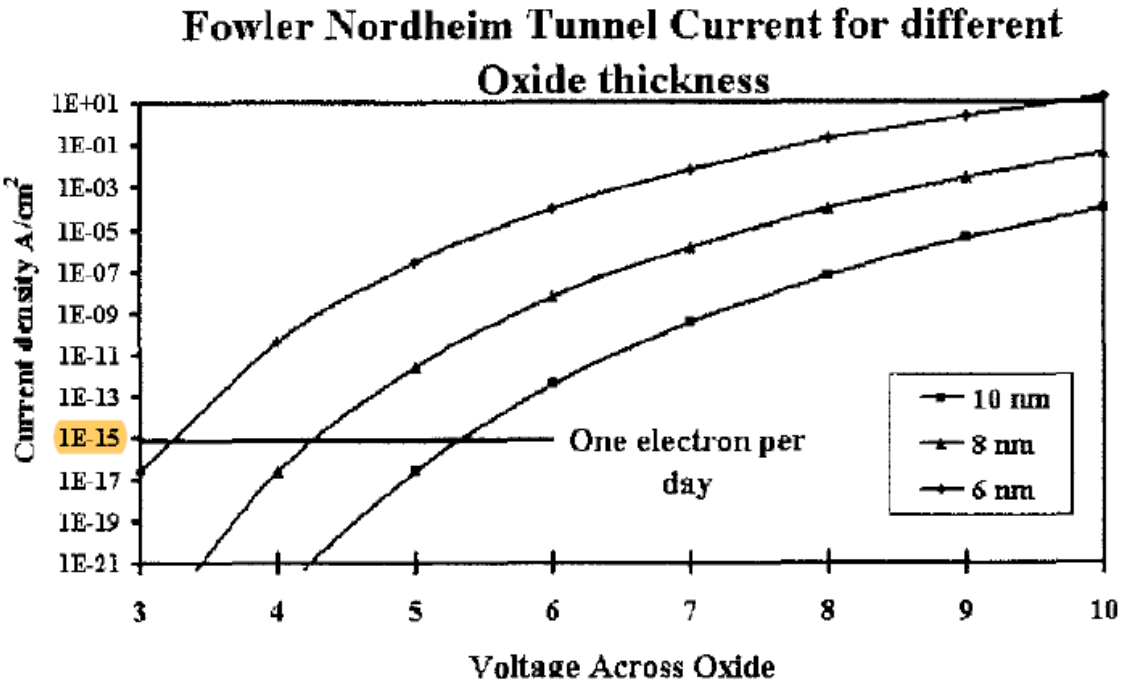
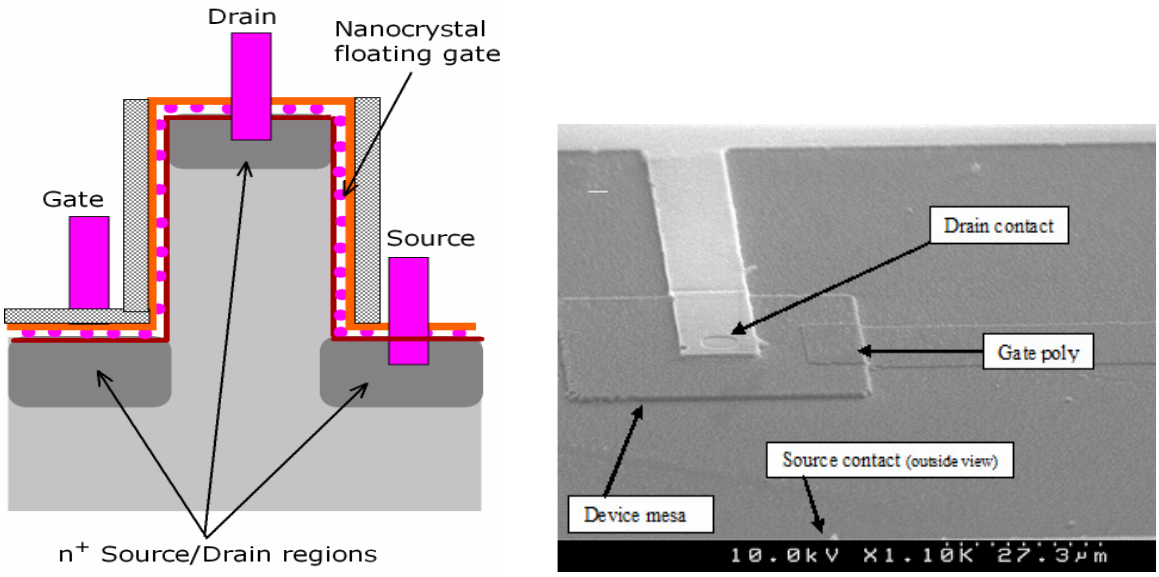


Figure 1.3: Tunnel oxide leakage current for different oxide thicknesses.[7] To guarantee a 10 year retention, an electron per day is allowable in a Flash transistor, while DRAM transistors can be 10^{13} times more leaky and logic transistors 10^{16} more leaky. Also, Direct Tunneling becomes significant beyond less than 8 nm of tunnel oxide thickness.

1.3 Vertical Flash memory transistor with nanocrystal floating-gate

One of the primary limiters of the integration density of Flash memory arrays that determine their capacity and cost-per-bit is the cell area of memory transistors, the other limiters being the peripheral circuits including the charge pumps, decoders and sense amplifiers. Faced with the aforesaid challenges to the scalability of the planar MOSFET device, three-dimensional and vertical transistors have been studied as an alternative cell design for over a decade in the realm of logic and memory applications, because of their inherently greater scalability and conduce for denser integration.[9–11] A vertical transistor is generally realized by suitably implanting an etched mesa or by etching epitaxially grown alternating p- and n-type layers to form vertically stacked drain, channel and

source regions. The gate-stack is then grown or deposited conformally around the mesa to encapsulate the vertical sidewall channel (fig. 1.4). The pillar-shaped vertical design is possibly best-suited especially for memory transistors since it allows the maximum physical and electrical scalability. This is because the channel width/length (W/L) ratio is nearly uniform for all cells in a dense memory array and has a more relaxed requirement compared with that of logic transistors constituting a complex circuit element. The following sub-sections discuss the advantages of a vertical design with nanocrystal floating gate for a Flash transistor, where the circumvention of the aforesaid three main challenges to planar Flash transistor scaling, viz. lithography, electrostatics and reliability, are explained in detail.

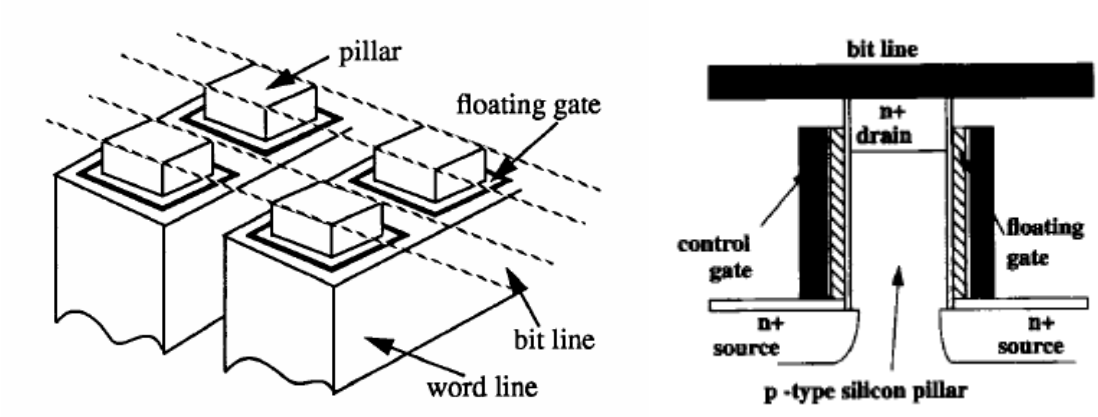


(a) (b)

Figure 1.4: (a) Schematic side-view of the vertical flash cell with nanocrystal floating-gate, (b) Scanning Electron Micrograph providing an isometric view of a fabricated cell.

1.3.1 Physical scaling and array design

With a vertical structure, each memory cell can be fabricated at the intersection of bit-lines and word-lines of an array (fig. 1.5). Therefore, with the mesa-width equaling the minimum line-width F of the available lithographic technology and isolated from its nearest neighbor cell by the same distance, the physical cell area can be scaled almost to the theoretical minimum of $4F^2$ sq. units (i.e. each cell occupying an area of $2F$ x $2F$ sq. units). Pein and Plummer demonstrated a cell area of 4.4 μm^2 (2 μm x 2.2 μm) by defining a mesa width of 1 μm with 1 μm lithographic capability, as they pointed out that physical scaling only aids and doesn't disadvantage the vertical design since the channel length is lithography independent.[10, 11] Pein *et al.* also pointed the way to implementing the vertical cell into an array with asymmetric cell separation along the word-lines and bit-lines – by closely spacing cells along word-line direction and depositing a sufficiently thick word-line polysilicon would close the gaps and form a continuous word-line. A slightly larger cell-spacing between adjacent word-lines ensures their isolation, after the polysilicon has been etched back. The bit-lines running perpendicular to the word-lines make contact to the transistor drain at the top of each mesa and their isolation from the word-lines is ensured by over-etching the word-line polysilicon causing it to lie a safe distance below the mesa top edge. Individual cells in an array do not need to have a separate drain contact; instead a trench can be etched along the planarizing dielectric exposing the mesa silicon and then filled with metal to form a continuous bit-line, thus not requiring any registration tolerance. Finally, they also noted that the "cross-point nature of the array simplifies peripheral circuitry, while the metal bit lines offer improved performance over virtual ground arrays where the bit-lines are long diffused regions".



(a) (b)

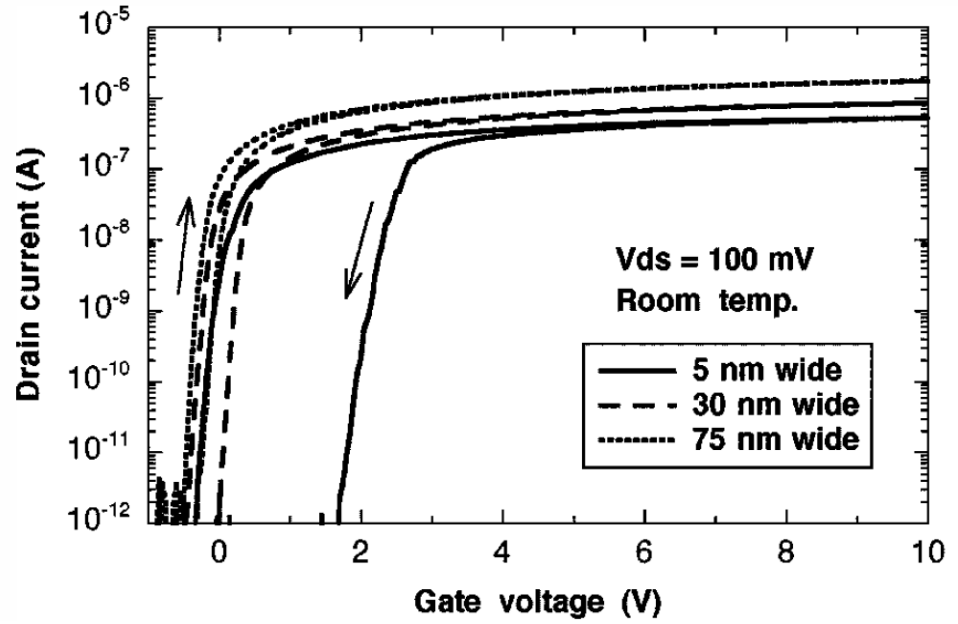
Figure 1.5: (a) Vertical Flash array design and (b) cell design with continuous floating-gate proposed by Pein *et al.*[10, 11] illustrating scheme for bit-line and word-line isolation and contacts.

1.3.2 Electrostatics

The gate-all-around (GAA) design of the vertical transistor can render maximum electrical coupling of the gate electrode in a fully-depleted and/or volume inverted body when the mesa width is scaled below ≈ 100 nm.[12, 13] This electrical scalability of the vertical architecture offers the advantages of low-threshold voltage, high transconductance or low sub-threshold swing and high drive current conducive to a low-power, high-performance transistor. Further, higher drive current is also contributed by the 4x (or, πx for a cylindrical mesa) physical device-width enhancement relative to a planar device from the sidewall-channels, while still minimizing the use of silicon real-estate. As already pointed out, the vertical cell can mitigate short channel effects by not necessitating any process/physical scaling of channel length with increasing integration density. At the same time, effective means of avoiding short channel effects, a necessity

in the case of stacked vertical devices in a NAND array, are virtues of the vertical design.[14]

Apart from the advantages of the vertical GAA structure, there can be electrostatic advantages derived from incorporating nanocrystal floating-gate therein. Saitoh *et al.* have demonstrated a significantly improved memory window and retention from tri-gate memory transistors with nanocrystal floating gate when scaled to sub-30 nm channel widths (fig. 1.6).[15] They have attributed the improvements to the so-called "classical bottleneck effect" and quantum confinement effects in the ultra-narrow channel (fig. 1.7). The classical bottleneck effect essentially results from the finite probability of few nanocrystals controlling the current flow in an ultra-narrow channel and Coulomb repulsive interaction of nanocrystals from opposite sides of the channel. The two dimensional quantum confinement of electrons in an ultra-narrow channel results in raising of occupied energy levels of electrons in the channel, leading to an improved data retention from reduced charge tunneling rates.



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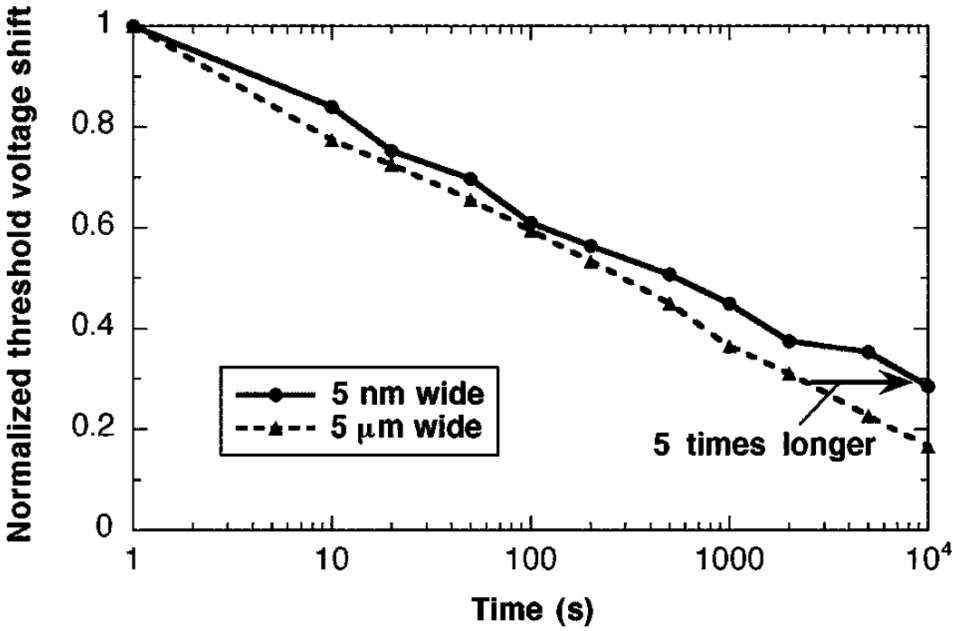
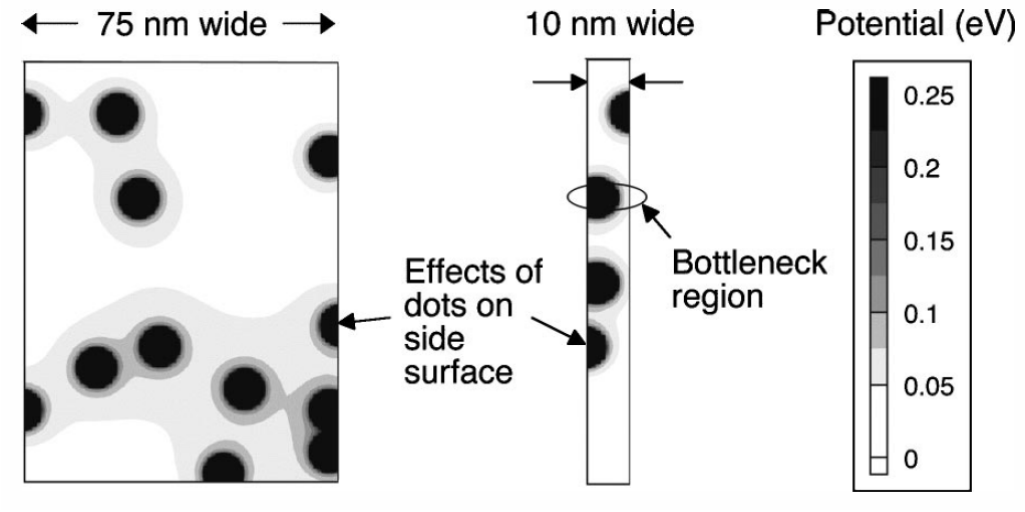


(b)

Figure 1.6: (a) Improved memory window in nanocrystal tri-gate transistors with ultra-narrow channel, and (b) improved retention (normalized to 1 s) resulting from scaling the channel to ultra-narrow widths.[15]



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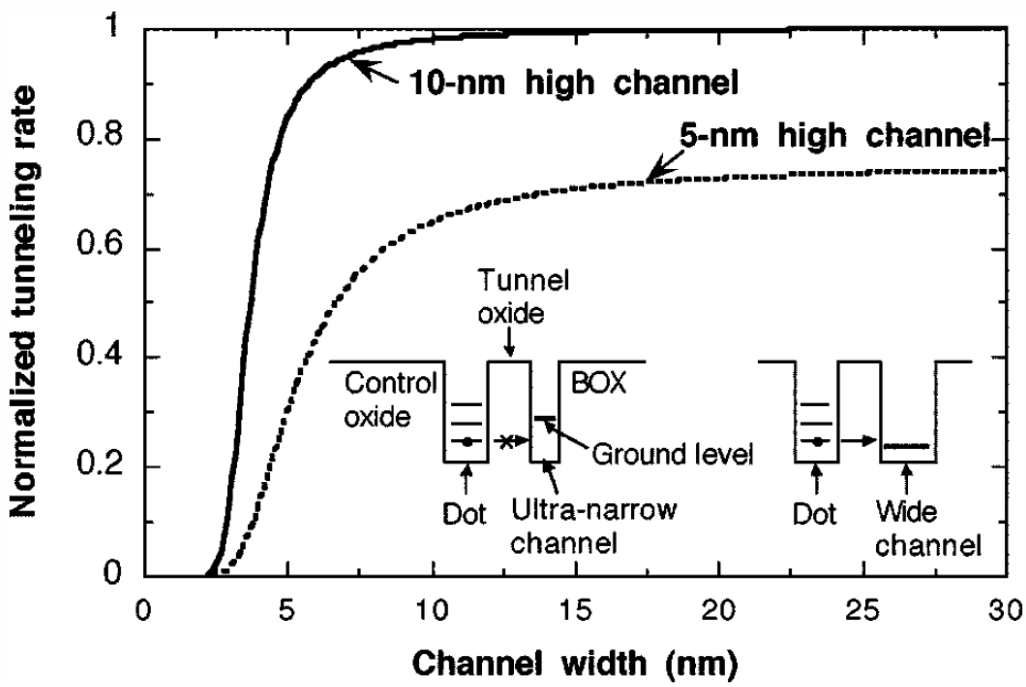


(b)

Figure 1.7: (a) Simulations of the "classical bottle-neck effect" more strongly affecting the potential in a 10 nm channel compared to a 75 nm channel, and (b) reduced tunneling loss from nanocrystals to ultra-narrow channel due to quantum confinement effects raising the channel potential.[15]

1.3.3 Reliability

The metrics of reliability of a non-volatile memory array are primarily retention and endurance. For Flash memory, retention is critically dependent on the thickness of the dielectric layers that encapsulate the charge-storing floating-gate. Thicker dielectrics can considerably reduce charge leakage, providing for enhanced retention. However, a thicker gate-stack also results in reduced electrical coupling between the control-gate, floating-gate and channel, impeding lithographic and electrostatic scaling of the transistor. Tiwari *et al.* proposed the idea of nanocrystals replacing the continuous polysilicon floating-gate in a Flash transistor, and several researchers have since espoused the benefits of discrete nanocrystals over continuous polysilicon for enhanced retention.[16] Freescale Semiconductors has also demonstrated nanocrystal Flash memory at 24 Mbit density with 90 nm technology node and operating at 6 V, for embedded applications.[17] The key advantages of a nanocrystal floating-gate can be summarized as follows:

- Each discrete nanocrystal storing one or more electrons ensures that unavoidable local defects due to process variations or damage from electrical stress in an ultra-thin tunnel oxide do not affect the memory state of a cell. Such oxide defects only result in leakage of charge stored in a few nanocrystals in the immediate vicinity of the weak-spot, leaving the memory state imtact.
- Nanocrystals with diameters of a few nanometers behave as quantum dots, with associated Coulomb blockade and quantum confinement effect on the stored charge, preventing leakage. The self-energy ($\sim\frac{e^2}{2C}$, C being the capacitance of the dot and $C = 2\pi\varepsilon d$, d being the diameter of the nanocrystal) of a quantum dot with 5 nm diameter encapsulated in SiO_2 matrix ($\approx$ 74 meV) is larger than the ambient thermal energy ($kT \approx$ 26 meV, at room temperature). Thus, quantum confinement

of stored electrons in the potential well of the nanocrystal conduction band (or even deeper traps) is effective for providing improved retention characteristics in spite of thinner tunnel and control dielectrics. Further, a lateral isolation of about 5 nm between dots prevents any intra-dot transport by Direct Tunneling.

- Discreteness of nanocrystals means that charge-storage is quantized, since only a certain number of electrons can be stored in the average number of nanocrystals making up the floating-gate of a sub-100 nm Flash cell. Further, quantized energy states coupled with the large self-energy of nanocrystals ensure a self-limiting charge injection into them, resulting in a saturating threshold shift of the memory cell.
- The manufacturing process can remain fully silicon compatible with a reasonable thermal budget. Researchers from Freescale Semiconductors have also noted that nanocrystal Flash simplifies the CMOS embedded process integration by requiring only 4 additional mask steps as opposed to the 11 necessary steps for continuous polysilicon Flash.[17]

Thus, nanocrystals seem poised to succeed the continuous polysilicon floating-gate in extending Flash memory to deep sub-100 nm devices. Part I of this dissertation is therefore based on the design, fabrication and characterization of a vertical Flash transistor with nanocrystal floating-gate with the hope that it can provide a platform for ultimate scalability of Flash memory technology. This work is pursued first by incorporating Chemical Vapor Deposited (CVD) silicon-germanium (SiGe) nanocrystals and next by improving on the nanocrystal ordering, density and size distribution by application of a technique of protein-mediated assembly of preformed and commercially available lead selenide (PbSe) nanocrystals.

1.4 Phase Change Memory

Flash memory technology has proved to be remarkably resilient in warding off threats from several competing non-volatile memory technologies such as magnetic random access memory (MRAM) and ferroelectric RAM (FeRAM) for several decades. Figure 1.8 provides a slightly dated technical comparison between the capabilities of various memory technologies that aim to compete or complement Flash in the non-volatile memory technology space. In the last few years Phase Change Memory (PCM) has proved to be viable in ultimately succeeding Flash as a mainstream and manufacturable non-volatile memory technology. Significant progress in developing PCM by Intel and ST Microelectronics, Samsung, Ovonyx, IBM and Infineon, Phillips Laboratories and others have propelled PCM from several decades of research to manufacturing potential, with a few of the aforesaid semiconductor manufacturers having demonstrated working prototype arrays between 128 to 512 Megabytes in capacity.[19, 20]

	Flash	CBRAM	FeRAM	MRAM	ORAM	PCRAM
Maturity	High Volume Product	Single Cells	Niche Products	Product Samples	Single Cells	Product Demonstrators
Density	4Gb	-	32Mb	16Mb	-	64Mb
Cell Size [um^2]	0.025	-	0.6	1.4	-	0.5
Embeddability	Yes	Yes	Yes	Yes	Yes	Yes
Nonvolatile	Yes	Yes	Yes	Yes	Yes	Yes
Random Read Access	80ns/10µs	<200ns	50ns	30ns	<200ns	50ns
Random Write Access	~10µs (erase 100ms)	<200ns	75ns	30ns	<100ns	50ns
Destructive READ	No	No	Yes	No	No	No
Write Endurance	10^6	$>10^5$	$>10^{12}$	10^{15}	10^5	$>10^{12}$
Write Voltage	Vdd+~10V	Vdd	Vdd	Vdd	Vdd+~2V	Vdd
Companies (Criteria: IEDM, ISSCC, VLSI publication during last 3 years)	Actrans Systems, eMemory Tech., Fujitsu, HaloLSI, Infineon, Intel, Macronix, Motorola, Powerchip, Renesas / Hitachi, Samsung, Sandisk, Sony, SST, ST, Toshiba		Agilent, Fujitsu, Hynix, Infineon Matsushita, Oki Ramtron Samsung Sanyo Toshiba TI	IBM Infineon Motorola NEC Renesas Samsung Sony	Infineon	Hitachi Intel Macronix Ovonyx Samsung ST

Figure 1.8: Comparison of emerging competitors to Flash technology (2004 data).[18]

The typical PCM cell essentially works based on the switching of a small volume of Germanium Antimony Telluride ($Ge_2Sb_2Te_5$ or, GST) alloy between high-resistance/amorphous (RESET) and low-resistance/crystalline (SET) states by Joule-heating from an attached heater. The GST material, heater and a selector device (such as a MOSFET, BJT or diode) together constitute a Phase Change memory cell. Phase Change materials such as the GST, generally from a group of compounds called chalcogenides, have been the subject of extensive research since the late 60's starting with the work of Stanford Ovshinsky,[21, 22] with a 256-bit array being reported by Neale, Nelson and Gordon Moore in 1970.[23] The PCM technology reported by Neale *et al.* had never entered manufacturing, however, because of material quality and power consumption issues. Chalcogenides are, however, currently in widespread use in rewritable compact disks (CD) and digital versatile disks (DVD±RW, DVD-RAM), where change in the phase of the material is effected by the direct heating from a laser beam.[24] However, even though the chalcogenides have been extensively studied over the last few decades, its application in an electrically switched non-volatile memory technology is new and therefore constitutes an area of active research and development.

The PCM cell is generally considered scalable to 10 nm or smaller with its figures of merit being not fundamentally physics limited with scaling, but instead limited by the manufacturing capabilities, such as available lithography technology.[25] In fact, unlike Flash technology, certain device characteristics such as programming current are expected to improve as the cell dimensions are scaled down in the case of PCM technology.[26] PCM also has inherent advantages of higher read/write/erase speed, direct over-erase, superior endurance and retention, radiation hardness and low voltage operation, apart from CMOS-process compatibility with reasonable thermal-budget allowance and cost competitiveness with Flash. On the other hand, fundamental

challenges to the PCM technology include size of the selector device which can potentially limit the scaling the overall cell size and array density, and the relatively high programming current that can lead to power dissipation and require complicated peripheral circuitry.

The research on PCM technology described in this dissertation is based on two fundamental metrics of non-volatility: operational cycles and data retention. It is demonstrated that a PCM cell and array is intrinsically improved with cycles of RESET operations, quite unlike almost any other semiconductor technology. Cell and array level electrical characterization and physical modeling of this phenomenon, collectively referred to as "seasoning" constitutes the latter part of this dissertation. Finally, a phenomenon of early and erratic data retention failure is studied on a large array to understand the underlying mechanism and methods of mitigation. This work was pursued on 180 nm and 90 nm PCM technology pursued by Intel Corporation and ST Microelectronics as a joint development project,[19] and constitutes Part II of this dissertation.

Part I: Extending floating-gate Flash memory with alternate cell design

CHAPTER 2

Vertical Flash Transistor with SiGe Nanocrystal Floating-gate

In this chapter, the design, fabrication and physical and electrical characterization of a three-dimensional, pillar-shaped Flash transistor with silicon-germanium (SiGe) nanocrystal floating-gate is described and discussed. The proof-of-concept device is demonstrated with a sidewall gate-stack including nanocrystal floating-gate made possible by conformal deposition steps.

2.1 Design, Fabrication/Processing and Physical Characterization

2.1.1 Vertical transistor

The Gate-All-Around vertical Flash transistor shown in fig. 1.4 was fabricated by photolithographic patterning and subsequent anisotropic reactive ion etching (RIE) rectangular mesas on 1 x 10^{15} cm^{-3} Boron-doped <100> Si wafers, so that the mesa sidewalls formed the channel with the drain at the top and source at the base of the mesa. The length of the vertical channel of the transistor is primarily determined by etch time, thus making the array integration density independent of channel length, unlike planar transistors. On the other hand, the channel width is the perimeter of the mesa, and as such, is a function of the lithography. However, as already mentioned, since the total

channel width is contributed by all four mesa sidewalls, the effective width is not nearly as constrained by lithographic scaling in the vertical device as it is in a conventional, planar Flash transistor. Mesas with various lengths, between 450 nm to 1000 nm were etched to form short-channel transistors with various channel lengths. It is worth noting that in the vertical transistors, the channel length is ultimately decided in conjunction with the source/drain depths, and therefore, the implantation energy.

The process flow is shown in fig. 2.1. Based on Synopsys® Taurus Process™ simulations, the junction depth/length in this batch of devices was tuned to about 200 – 250 nm, producing channel lengths ranging between 200 nm and 900 nm for the same devices. To minimize the unavoidable surface roughness on the sidewalls from RIE, a sacrificial dry thermal oxide 4 – 10 nm in thickness was grown. For the processing of devices described in this chapter, a sacrificial, protective layer of silicon nitride was also deposited by low-pressure chemical vapor deposition (LPCVD) to protect the sidewall channel during the subsequent source/drain implantation step. This nitride layer was then anisotropically etched (RIE) to expose the source/drain regions for implantation. The wafers were then implanted with Phosphorus ions, with an energy of 15 – 20 keV, dose of 1 x 10^{15} cm^{-2}, 7 ° tilt and 90 ° rotation. It may be noted that the implantation parameters used for these devices are similar to the "standard" parameters used for planar MOSFET processing in our research group, except for slightly lower energy of implantation (which tends to be 25 – 30 keV for planar devices), and the rotation incorporated for implanting all four sidewalls equitably. Following the implantation step, the protective nitride layer and the underlying sacrificial thermal oxide layer were removed with orthophosphoric acid and dilute 5 % hydrogen fluoride dissolutions, respectively. Subsequently, conformal growth of the gate-stack layers on the mesa sidewalls included a 4.5 nm-thick dry, thermal tunnel-oxide grown at 850 °C, Rapid-

Thermal CVD (RTCVD) grown SiGe nanocrystals and 15 nm-thick LPCVD control-oxide deposited at 520 °C. A polysilicon layer was then deposited by LPCVD at 850 °C, implanted again with Phosphorus having 30 keV energy, 1 x 10^{15} cm^{-2} dose, 7 ° tilt and 90 ° rotation, and etched to form the control-gate electrode. After depositing an isolation oxide and patterning and etching gate electrodes, electrical contacts to the drain at the mesa top, source at the mesa base, substrate (body) at the wafer backside and sidewall gate were finally formed by aluminum sputtering.

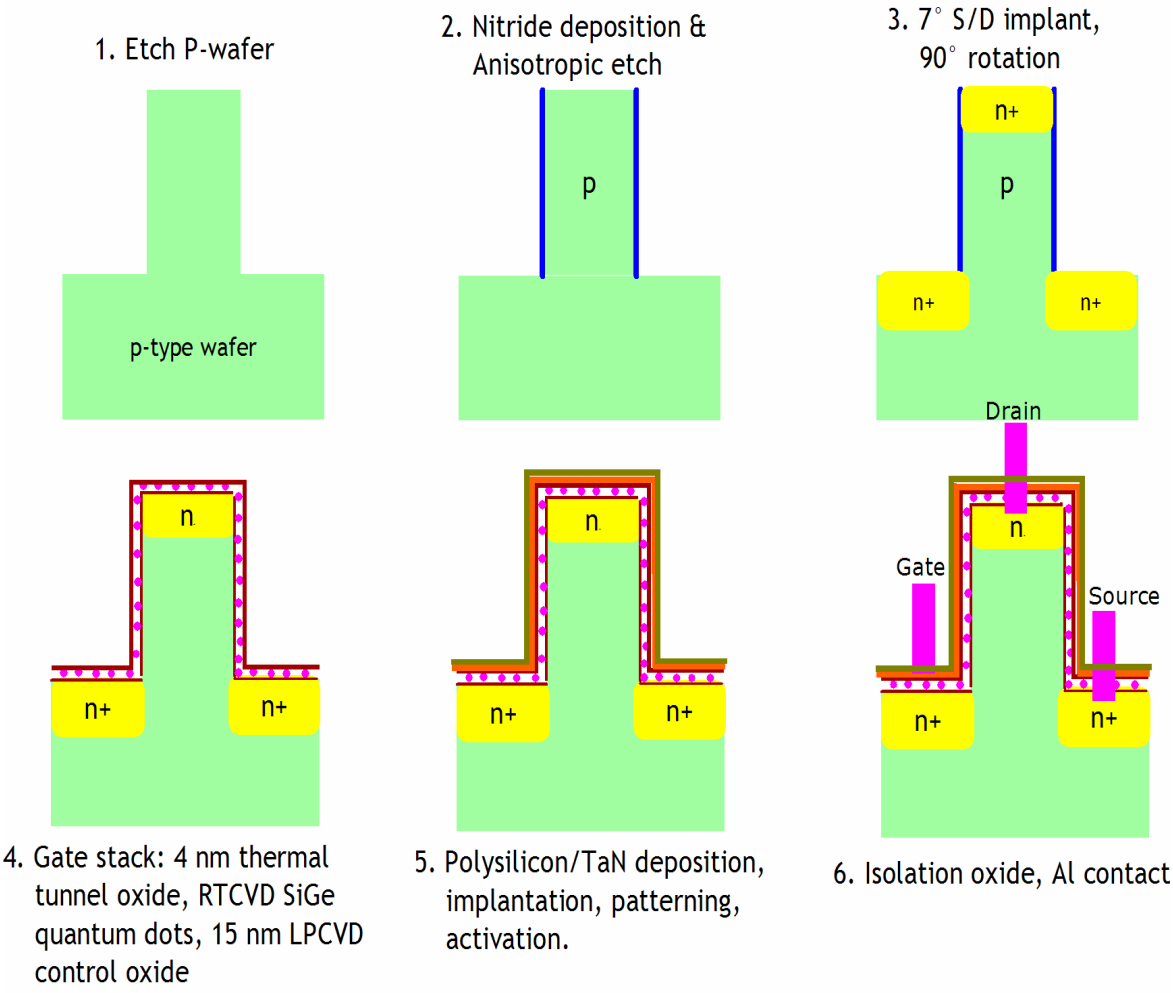


Figure 2.1: Process flow for fabrication of vertical Flash transistors with SiGe nanocrystal floating-gate.

2.1.2 Silicon-Germanium nanocrystal floating-gate

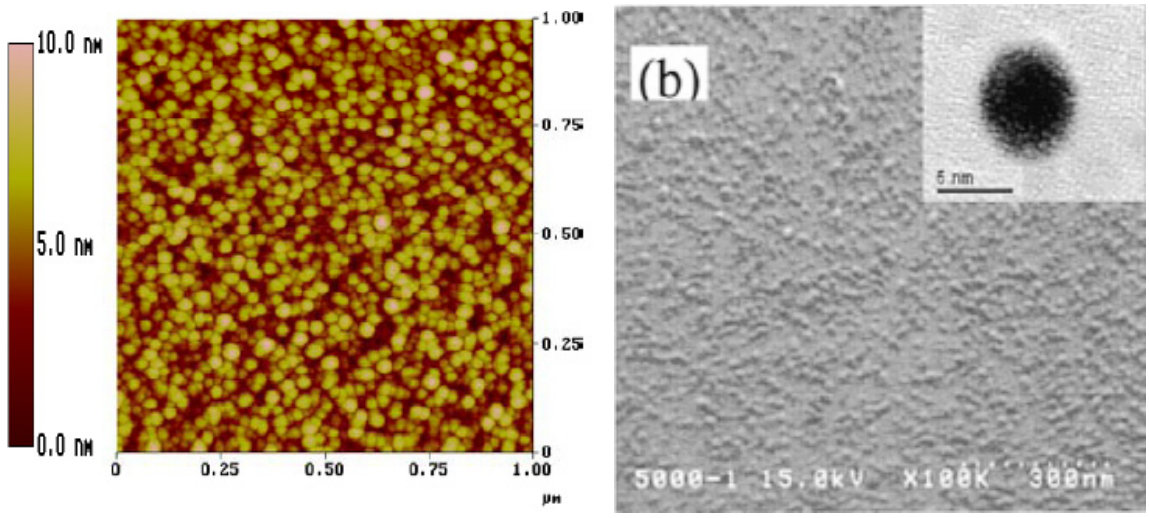
The nanocrystal floating-gate incorporated in vertical Flash transistors described in the previous section was grown by Volmer-Weber nucleation in a custom-made RTCVD system.[27, 30] SiGe nanocrystals used in this process lend themselves particularly well to a manufacturing environment by virtue of being fully silicon compatible and requiring a low thermal budget. Since SiGe has a smaller band-gap compared to Si, electrons are stored in a relatively deeper potential well of the SiGe conduction band, contributing to superior retention properties.[28] The higher dielectric constant of SiGe compared to Si also mitigates concern about smaller nanocrystals having too high a charging energy in a memory cell, which can be an impediment to electrons being efficiently "injected" inside nanocrystals during programming operations.[29] On the other hand, difficulty of growing pure Ge nanocrystals on amorphous substrates due to higher surface energies and lower evaporation temperature of Ge relative to Si make SiGe a particularly attractive compromise as the semiconductor material of choice for nanocrystals in a Flash memory cell.[28, 31] The nanocrystals for the devices described in this chapter were grown using nearly identical processes and recipes characterized in detail and optimized by Dong-Won Kim *et al*.[30-32] Thus, the growth process parameters had been optimized for a maximum attainable nanocrystal density of the order of 10^{11} cm^{-2} and a nanocrystal diameter between 7 and 10 nm (fig. 2.2), with a nanocrystal composition of 16 % Ge in Si. In brief, the growth chamber conditions involved high purity GeH_4 and Si_2H_6 gas flow at a substrate (wafer) temperature of ~ 520 °C. During growth, the chamber pressure was 600 mTorr. The gas flow sequence involved an initial flow of H_2 gas, followed by Si_2H_6 and finally GeH_4 (GeH_4:Si_2H_6 :: 3:4), with each gas flow being held constant while the next one was added to the mix, for a combined 90 s of nanocrystal growth time. The pre-treatment of the SiO_2 surface with H_2 and Si_2H_6 before

GeH_4 flow had been shown to cause a 3.5x increase in the nanocrystal density that was attributed to a higher tendency of Si_2H_6 to nucleate on the SiO_2 surface.[31] The most likely atomistic mechanism of SiGe nanocrystal growth on the Si surface has been cited as the following:

$$Si_2H_6(g) + 2* \rightarrow 2SiH_3(s) + nGe(s) \rightarrow 2Si(s) \quad [1]$$

$$GeH_4(g) + * \rightarrow GeH_4(s) \rightarrow Ge(s) \quad [2]$$

where * is a vacant site of nucleation on the surface and n is a constant.[30] The dependence of the dot density on time and substrate temperature, and GeH_4 to Si_2H_6 ratio is reproduced for reference in fig. 2.3 and fig. 2.4, respectively.



(a) (b)

Figure 2.2: (a) Atomic Force Micrograph, and (b) Scanning Electron Micrograph[32] of SiGe nanocrystals grown by RTCVD with a density of 10^{11} cm^{-2}, characterized on a planar surface.

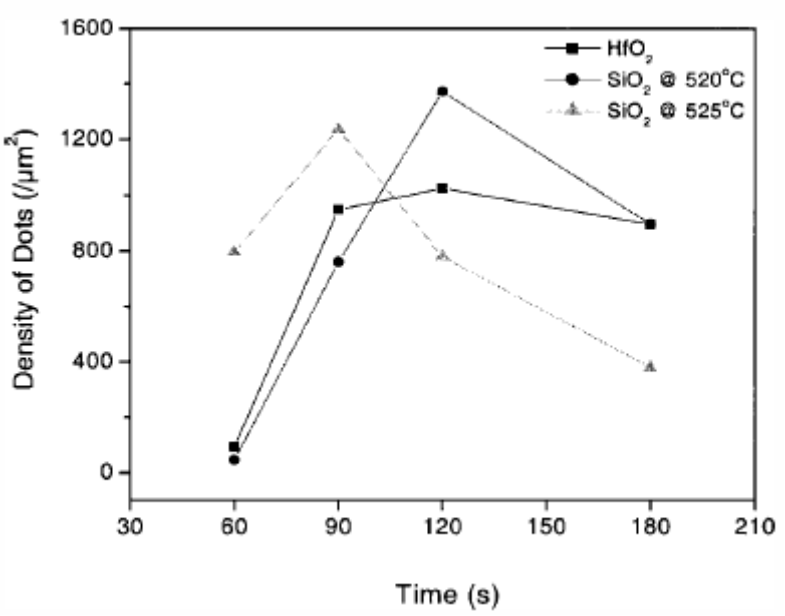


Figure 2.3: Dependence of SiGe nanocrystal density grown by RTCVD on time and substrate temperature.[30]

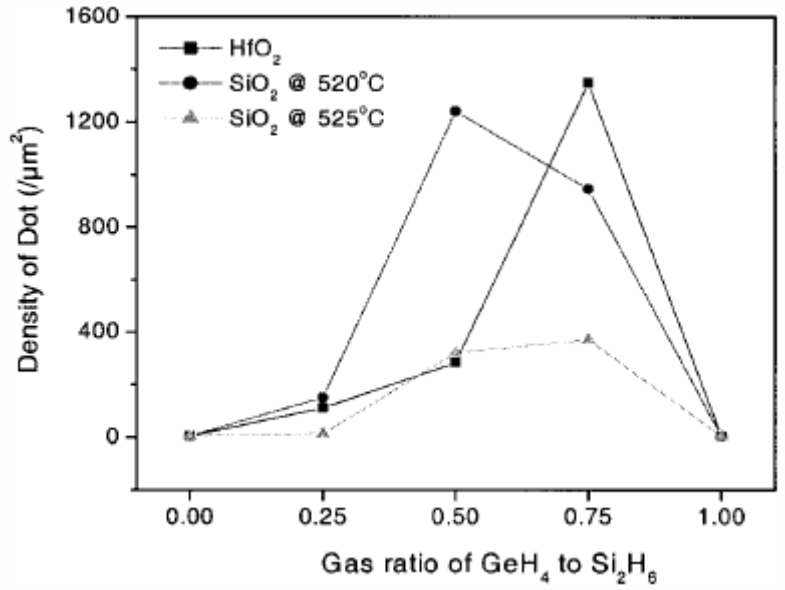


Figure 2.4: Dependence of SiGe nanocrystal density grown by RTCVD on ratios of GeH_4 to Si_2H_6 gas.[30]

Physical characterization of the deposited nanocrystals, shown in fig. 2.2, was performed on a planar surface due to the fact that scanning probe characterization methods cannot be easily and reliably applied on the vertical sidewalls. On the other hand, the deposited semiconductor nanocrystals were not clearly contrasted against the backdrop of SiO_2 tunnel-oxide when seen under the available Scanning Electron Microscopes with a tilted stage. With the understanding that Volmer-Weber growth process is not affected or driven by gravitational forces, the nanocrystal self-assembly process is expected to proceed very similarly on the vertical sidewalls as on a planar surface, yielding a very similar nanocrystal density, distribution and size. This expectation has been recently vindicated by Kim *et al.* who were successful in imaging nanocrystals on the fin sidewalls of a nanocrystal FinFET transistor, as shown in fig. 2.5.[33] They noted that any difference in the density of nanocrystals on sidewalls can only be attributed to any difference in the level of exposure to the lamp supplying the surface diffusion energy for the nucleation of the adatoms. Also, it is worth noting that while the tunnel-oxide thickness was adjusted for higher growth rates on the <110> sidewall surfaces, the growth of nanocrystals on oxidized surfaces were not affected by the sidewall crystal orientation. Figure 2.6 shows the vertical cross-sectional Transmission Electron Micrograph of a fabricated vertical Flash cell with the different material layers, as described in this chapter.

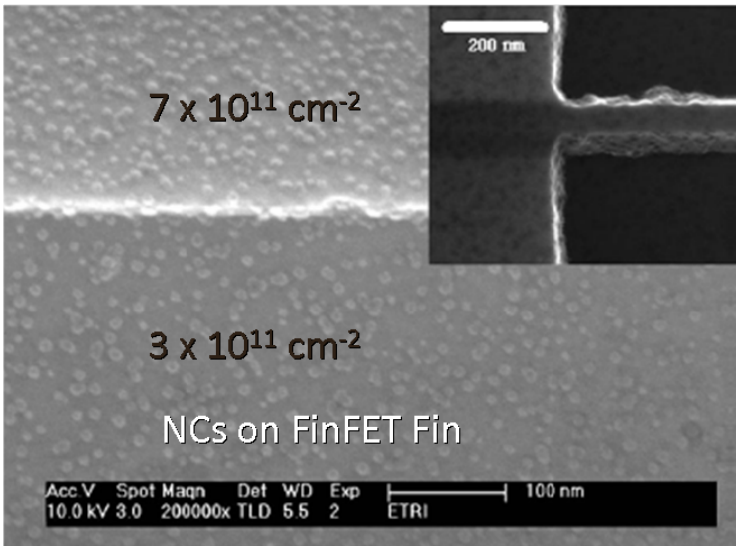


Figure 2.5: Nanocrystals deposited on the top and sidewall of the fin of a FinFET Flash memory cell.[33] The difference in the density of nanocrystals between the planar top and vertical sidewalls was attributable (only) to the different amounts of exposure to the energy from the lamp driving the Volmer-Weber nucleation process.

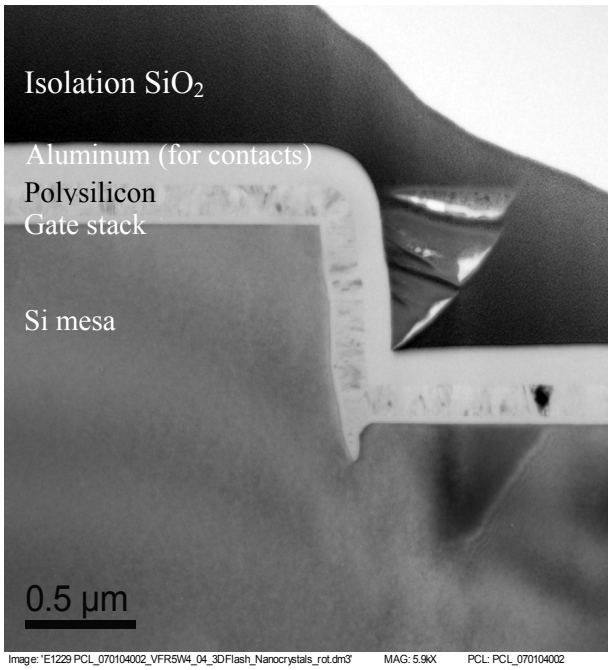


Figure 2.6: Cross-sectional Transmission Electron Micrograph of a vertical cell, showing the different layers of comprising materials (courtesy: Domingo Garcia, ATDF, International Sematech, Austin, TX).

2.2 Electrical Characterization

The electrical characterization of devices fabricated as described in the previous sections included transconductance ($I_D - V_G$) and output ($I_D - V_D$) characteristics, to verify the operation of the basic transistor. The memory window was ascertained together with the transconductance characterization, as shown in fig. 2.7.

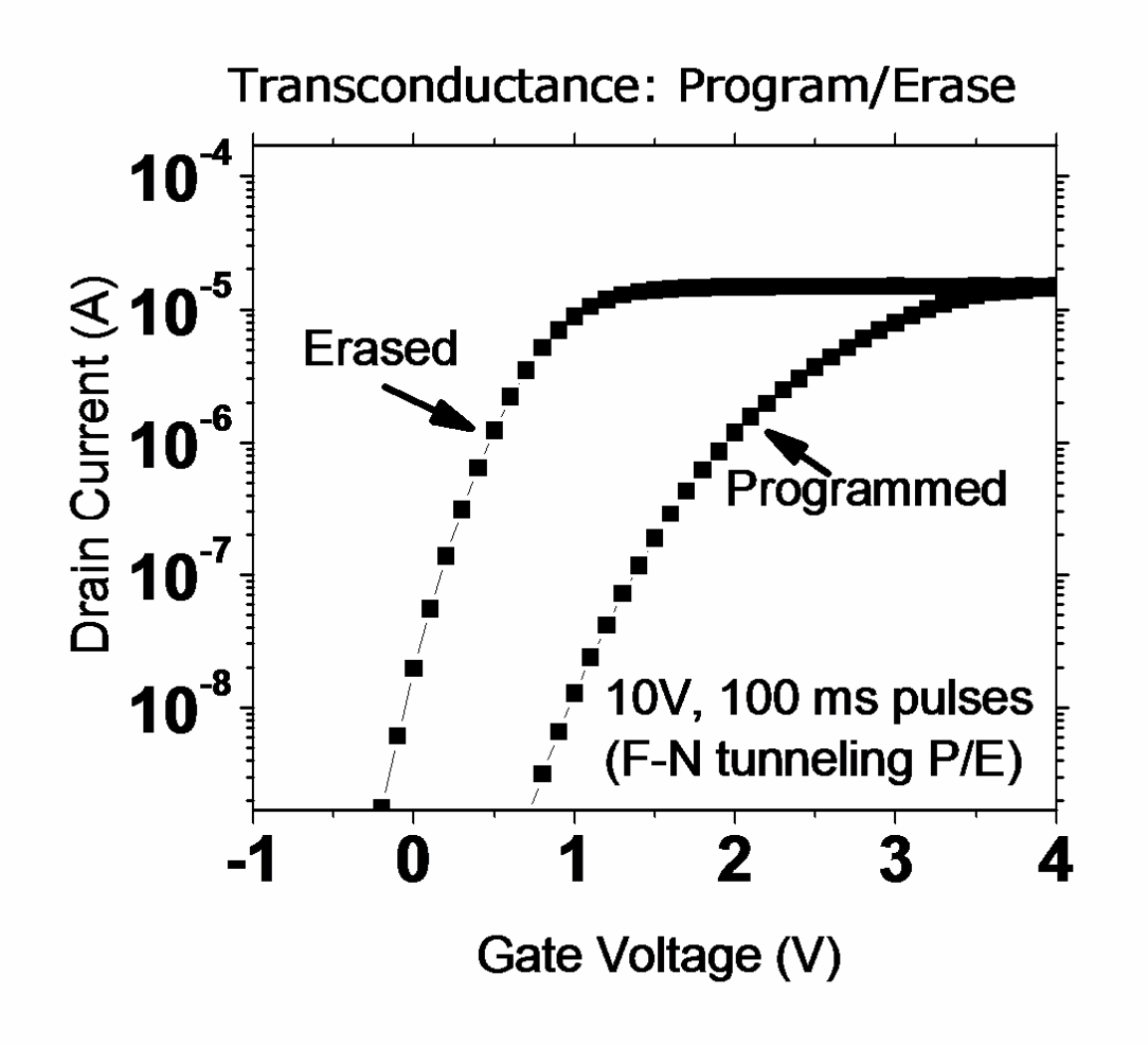


Figure 2.7: Transconductance characteristics of transistor and memory window for short-channel devices (mesa height = 0.9 μm, width = 30 μm, T_{Tox} = 4.5 nm, T_{Cox} = 15 nm).

The use of Fowler-Nordheim (F-N) tunneling of charge lends itself particularly well for efficient programming as well as erasure of nanocrystal Flash transistors since the mechanism results in uniform charge transfer across the gate-area. On the contrary, hot-electron injection mechanisms result in charge storage either in drain or source end of the channel, since the discrete nature of nanocrystals prevent any lateral re-distribution of charge. Thus, for the proof-of-concept devices discussed in this dissertation, Fowler-Nordheim tunneling was used for programming and erasure.

As shown in fig. 2.7, the memory cell was programmed by applying ± 10 V pulses of 100 ms width at the gate electrode with the source, drain and body contacts floated. The consequent tunneling of electrons from the channel to the nanocrystal floating gate resulted in distinct memory states separated by at least 1 V. Control devices fabricated in the same manner except lacking nanocrystal deposition showed a hysteresis of ~ 0.1 – 0.2 V under the same program/erase conditions, most likely due to interfacial and bulk charge trapping. A larger memory window could be extracted with larger pulse amplitude or width; however, that usually led to compromised endurance characteristics. An investigation of the CVD control-oxide quality by measuring Capacitance-Voltage curves of fabricated MOS-capacitors had revealed the presence of large density of fixed charges within the oxide. This suggested that the poor quality of the oxide compromised the performance of the devices somewhat – a fact also reflected in the endurance and to a lesser extent, retention characteristics of the device. The ouput characteristics of the transistor reported in fig. 2.8, also show reasonable behavior except for evidence of a Schottky-like behavior at low voltages, which can be attributed to less-than-perfect metal (aluminum) to semiconductor (silicon) contacts at the electrodes due to Fermi-level pinning effects.

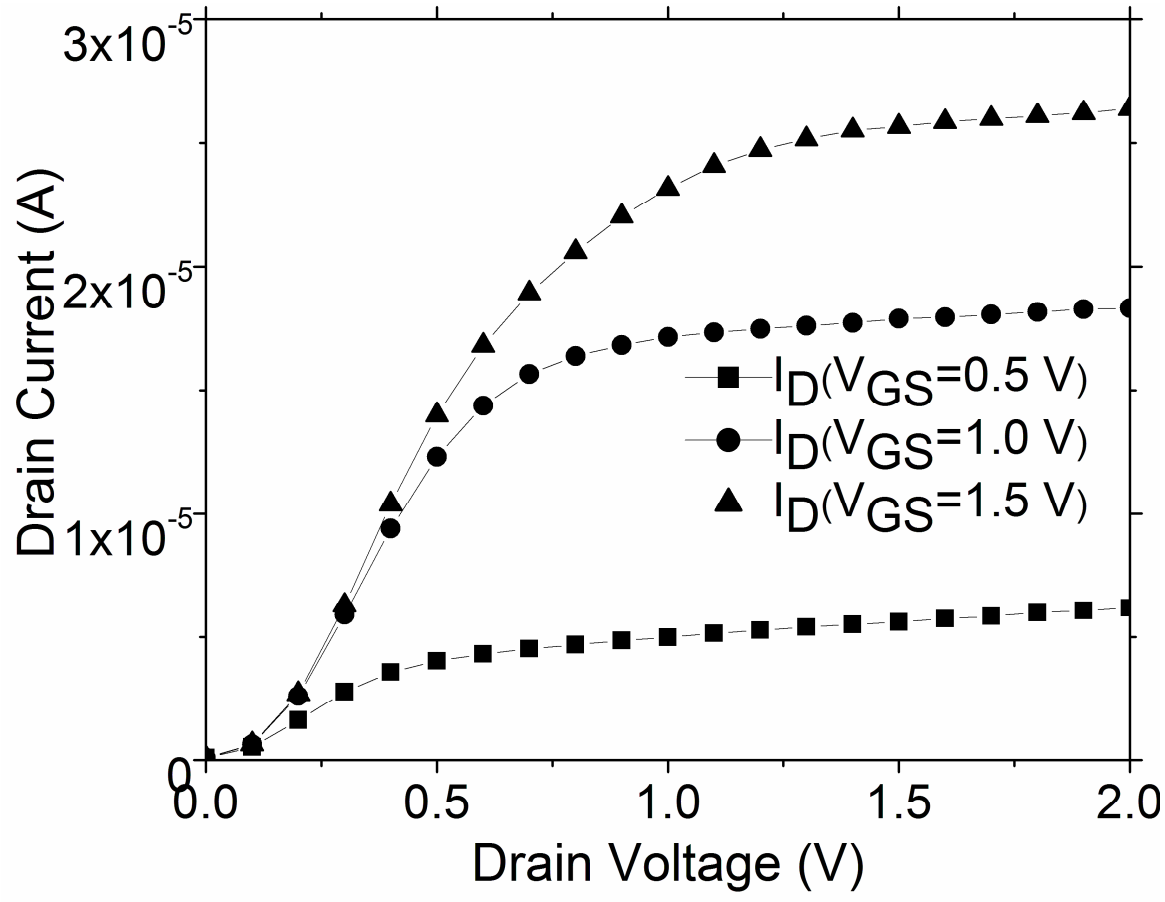


Figure 2.8: Transistor output current characteristics (mesa height = 0.9 μm, width = 30 μm, T_{Tox} = 4.5 nm, T_{Cox} = 15 nm).

The endurance characteristics are reported in fig. 2.9, which shows the device retaining an open memory window up to 10^5 cycles of operation. As evident from the figure, both the erased and programmed states show an upward drift through the endurance cycles. This is a trend reported by several researchers, who have attributed the phenomenon to the finite cross-section of nanocrystals. In the case of nanocrystal floating-gate, the discrete nature of nanocrystals (as opposed to a continuous floating-gate of polysilicon or silicon nitride) implies that a significant portion of the tunneling current from the channel during programming operations is inevitably "dissipated" through the control-oxide. In

fact, the programmed memory state is considered saturated when the programming current through the tunnel-oxide equals the current dissipated to the control-gate through the control-oxide. Owing to the deep level of traps thus formed and occupied, the erase operation is unsuccessful in de-trapping the trapped electrons in the control-oxide. Therefore, electron trap formation and occupation in the control oxide can happen as a cumulative effect of programming, especially in the case of less-than optimum control-oxide quality. As mentioned before, the known non-optimized quality of CVD control-oxide of these reported devices is the most likely reason for the gradual but significant increase of programmed as well erased threshold voltages in the endurance tests. This argument is vindicated by "industrial-grade" nanocrystal floating-gate devices and arrays reported by Freescale Semiconductors.[17]

Recent work by Irrera and Puzzili has shown that successive, repetitive square-wave pulses used for F-N tunneling program/erase endurance measurement stresses the oxide and leads to the generation of traps leading to Stress-Induced-Leakage-Current (SILC), degrading the memory reliability.[34] They have also shown that memory window movement and closure can be mitigated by optimizing the pulsing scheme of the endurance testing. They have also found that the generation of a trap is a two-step process with each step having a finite time.[35] The first step is the generation of trap precursors due to applied stress and if the stress continues, as a following step, the precursors convert to stable traps that increases SILC and permanently degrades the oxide. However, if the stress is switched off during the second step before the precursor converts to a stable trap, then the precursor spontaneously anneals instead, and permanent damage to the oxide is avoided. Irrera *et al*. have suggested that the time-scale of the first step should be less than 500 ns to prevent formation of permanent traps, while the precursors should be allowed to anneal for more than 10 μs. Thus, introducing a period of gap or

annealing time between each program and erase pulses of endurance testing can lead to spontaneous "healing" of the trap pre-cursors, leading to significantly reduced oxide degradation during repeated pulses. Their experimental data with the modified pulsing has shown improvement against memory window movement and closure, when compared with conventional pulsing (fig 2.10). Thus, the endurance characteristics described in fig. 2.9, which was tested with the "standard cycling" devoid of any annealing time for mitigation of permanent trap formation, is most likely a consequence of the abovementioned oxide degradation over and above its intrinsic poor quality, rather than the vertical architecture.

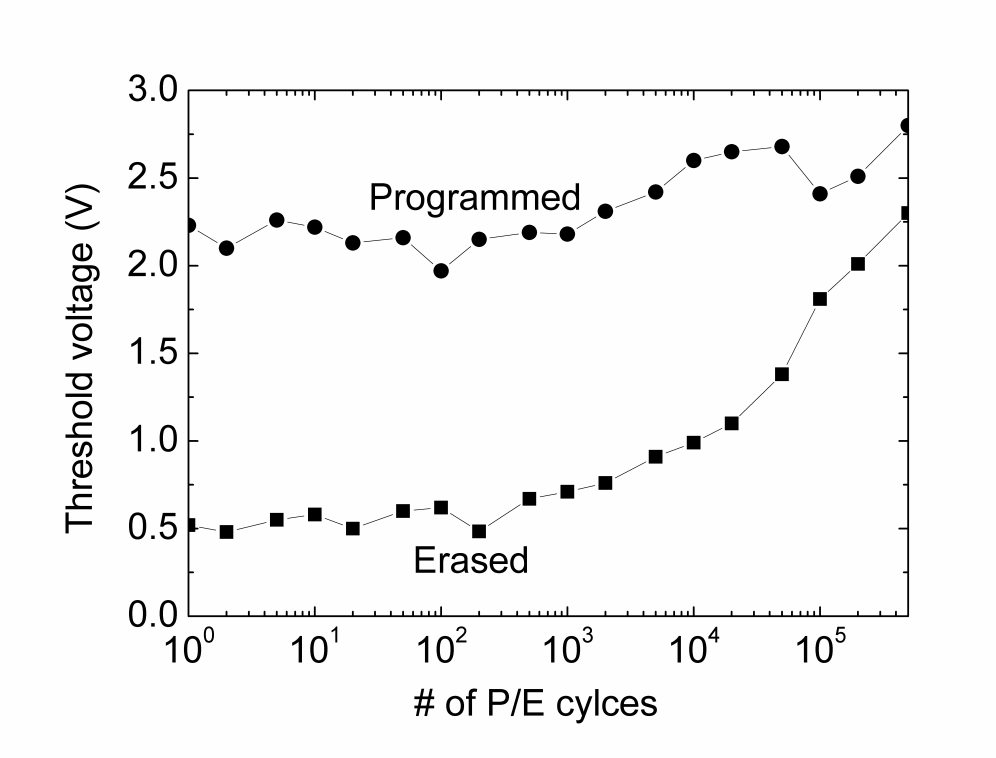
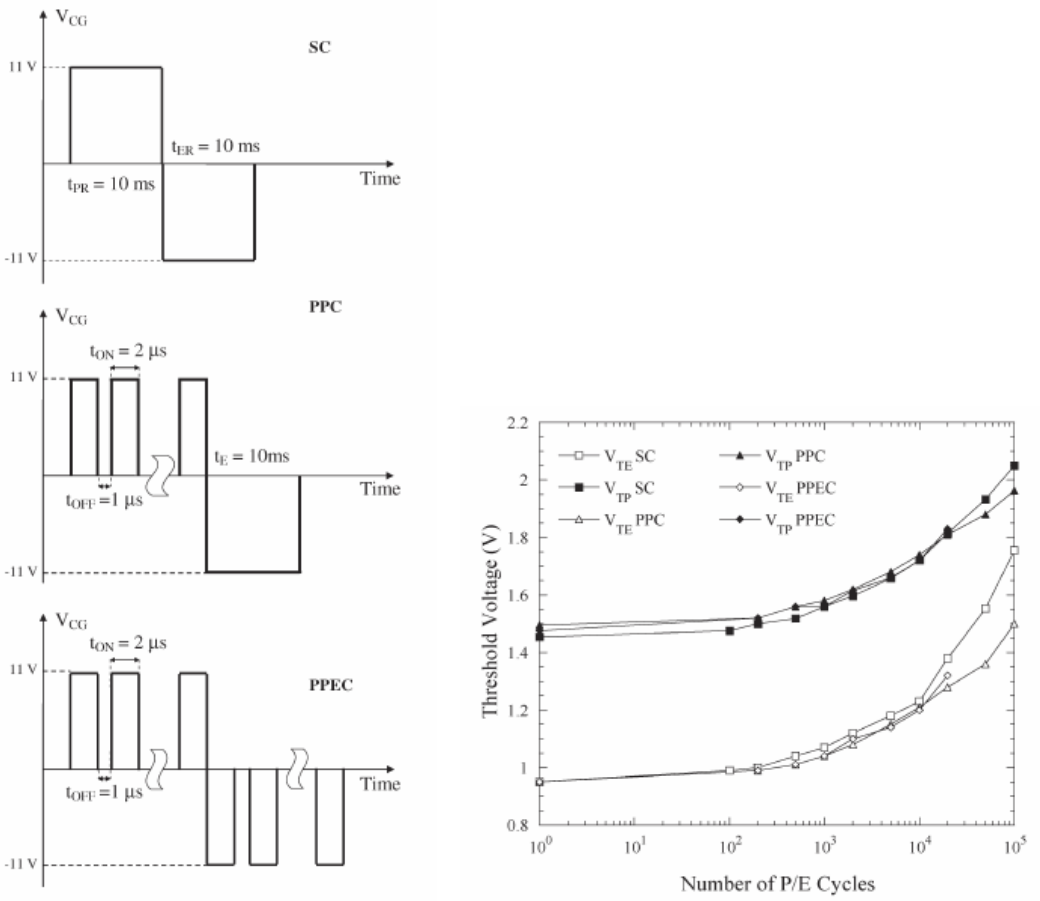


Figure 2.9: Endurance characteristics over 10^5 cycles. ± 10 V, 100 ms F-N tunneling program/erase was used for each cycle. The relatively higher pulse amplitude used, while maximally stressing the device, was most likely also responsible for electron trapping in the control oxide, causing the relatively higher threshold voltages.



(a) (b)

Figure 2.10: (a) Proposed modified pulsed program and erase schemes by Irrera *et al.* and (b) improved endurance characteristics of nanocrystal Flash memory, for comparison with fig. 2.9.[35]

The retention characteristics of the memory cells is shown in fig. 2.11, both at room temperature and at 85 °C, indicating a 10-year retention survival. The minor instabilities seen in the programmed and erased state threshold voltages is most likely noise arising from the measurement apparatus and/or minor trapping and de-trapping of electrons occurring in the gate dielectric layers.

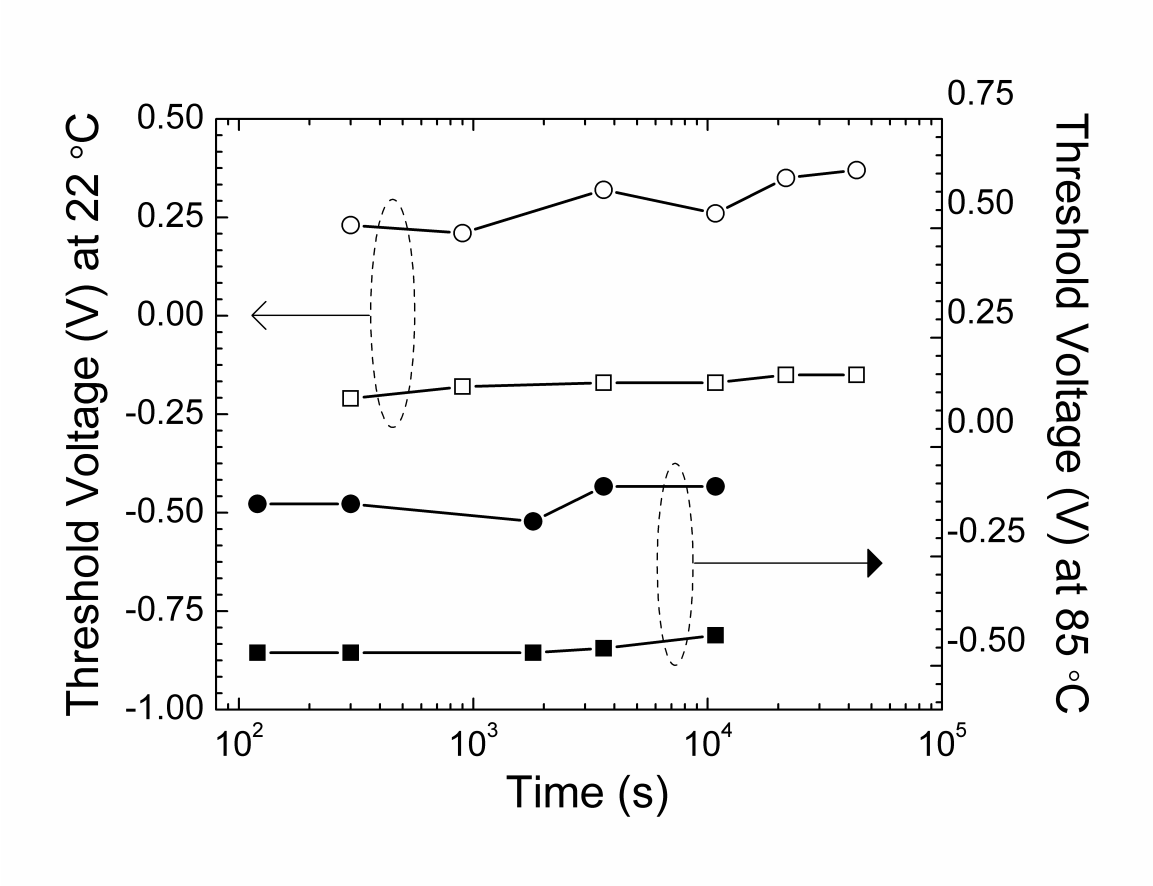


Figure 2.11: Retention characteristics at room temperature (left axis, hollow symbols) and at 85 °C (right axis, solid symbols) showing a robust memory window exceeding 10 years.

The vertical/pillar transistor described in this chapter can be fabricated by two different approaches. The other method is epitaxial growth of the source, channel and drain layers by Ultra High Vacuum Chemical Vapor Deposition (UHVCVD) with appropriate composition (possibly incorporating SiGe) and doping of the layers, followed by RIE to realize the mesa structure. While this method allows engineering the doping and composition profile for especially short-channel transistors ($L_{Channel} \approx 100 – 200$ nm) and can eliminate any requirement for implantation when used with a metal gate, the epitaxial growth usually produces poor crystalline quality for thicker layers ($L_{Channel} \approx$

500 – 1000 nm) corresponding to longer channel devices. A requirement on the source/drain layers to be at least 100 nm thick in order that spiking from the aluminum metallization is avoided, further increases the epitaxial growth time necessary in the UHVCVD chamber. Poor quality of epitaxial growth and crystalline quality was observed for layers thicker than ≈ 200 nm, evidenced by greatly increased surface roughness (fig. 2.12). However, for a Flash transistor requiring a longer channel length relative to a logic device, and with the vertical design being relatively independent of channel length from the perspective of integration density, the process flow with implantation appears adequate.

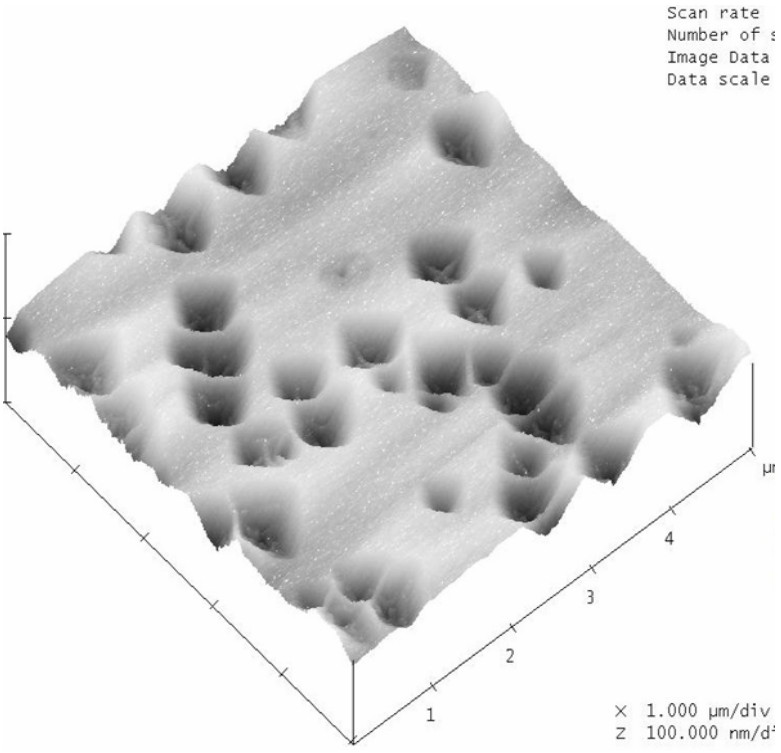


Figure 2.12: Atomic Force Micrograph of surface of Boron-doped Si epitaxial layers grown thicker than 200 nm by Ultra-High Vacuum Chemical Vapor Deposition showed poor crystalline quality.

In summary, a vertical, three-dimensional Flash transistor with sidewall nanocrystal floating-gate was designed, fabricated and characterized as a means of mitigating the scaling and integration density limitations of the planar Flash memory cell. While there is room for improvement and optimizations in the processing, the key figures of merit of the basic transistor as well as that of the memory cell were described, demonstrated and discussed in this chapter.

CHAPTER 3

Vertical Flash Memory with Protein-mediated Assembly of PbSe Nanocrystal Floating-gate

A novel technique of protein-mediated assembly of the nanocrystal floating-gate, developed in our research group for obtaining an ordered array of uniformly-sized preformed nanocrystals, was applied to the vertical Flash memory architecture to enhance its scalability and manufacturability. Extensive physical and electrical characterization of the fabricated devices, together with process improvements for the vertical transistor resulting in improved electrical performance, are described and discussed in the following sections.

3.1 Design, Fabrication and Physical Characterization

3.1.1 Protein-mediated assembly of nanocrystal floating-gate

While it is generally acknowledged that a nanocrystal floating-gate can enhance the reliability characteristics of Flash memory transistors with tunnel-oxide thinner than ~ 8 nm, thereby also enhancing the scaling possibilities of the transistor, a common remaining argument is the lack of microscopic control over the size and ordering of nanocrystals.[36, 37] Traditional nanocrystal growth or deposition techniques have involved Physical Vapor Deposition,[38] Chemical Vapor Deposition,[28] aerosol[39] and precipitation of

nanocrystals from ion implanted and Si-rich oxide layers.[40] The mechanics of these processes, such as Volmer-Weber nucleation in case of Chemical Vapor Deposition, usually precludes any fine microscopic control over the atomistic growth processes, which leads to variations in size and ordering of the nanocrystals. Thus, for devices scaled to gate-lengths below ~ 25 nm, where each memory cell would contain less than 10 nanocrystals, there can be a significant variation in the number of nanocrystals and consequently, the threshold voltage across cells in a dense array. Also, since the growth and assembly are unified in these traditional processes, the choice of material system for the nanocrystals becomes limited. Therefore, the prospects of nanocrystal Flash memory is often considered limited in scaling, especially in the context of high-volume manufacturing where threshold voltage spread across array cells can lead to severe yield and reliability concerns.[37]

Owing to the abovementioned concerns, several avenues of research have been undertaken over the last few years to gain control over and improve upon the size distribution and ordering of nanocrystals. Most notably, IBM Research has pioneered the use of di-block copolymers for templated self-assembly of nanocrystals for Flash memory applications.[41] While such templated assembly of nanocrystals by the use of copolymers produce very good size uniformity and spatial distribution (fig. 3.1), the nanocrystals are quite large (20 nm), with large separation (40 nm) and consequent sparse density (6.5 x 10^{10} cm^{-2}) due to inherent properties of the copolymer assembly process. For exploiting the nanoscale properties of the nanocrystals such as quantum confinement and Coulomb blockade, the optimal size of nanocrystals for use as Flash memory floating-gate is considered to be 4 – 7 nm, with an inter-particle separation of ~ 5 nm so that the optimum particle density of ~ 10^{12} cm^{-2} can be achieved. Hence, several researchers have recently explored biologically inspired self-assembly techniques,

exploiting properties of deoxyribonucleic acid (DNA), virus or protein molecules as the mediators of the nanocrystal assembly process.[42] However, not all of these templated

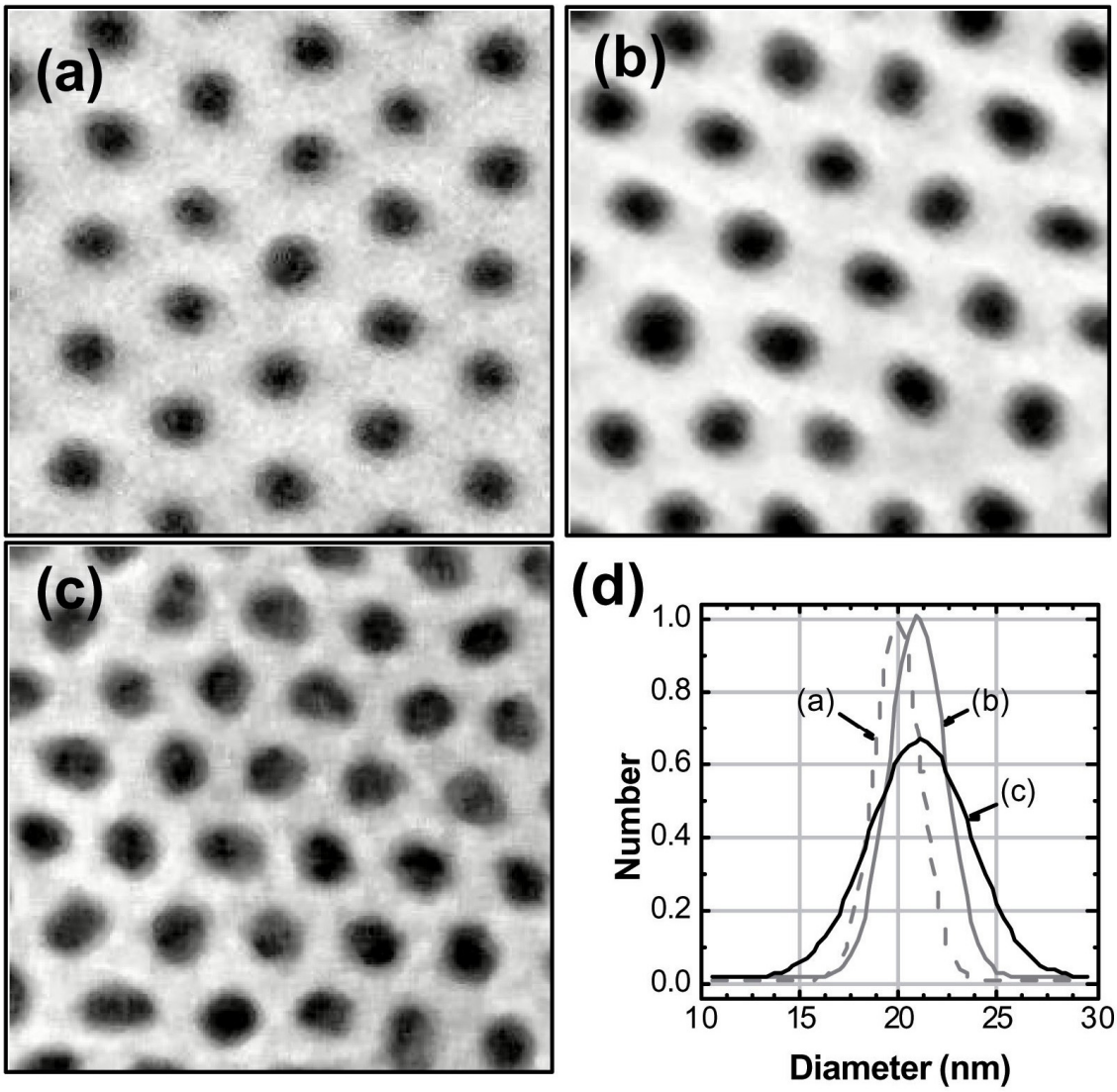
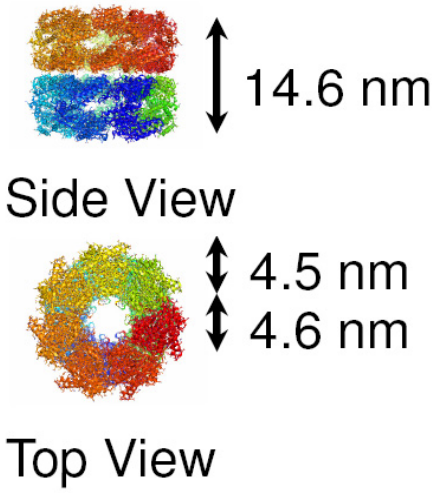


Figure 3.1: Copolymer-assisted nanocrystal self-assembly process pioneered by IBM Research.[41] (a) Ordered polymer-based template for nanocrystal assembly, with pore sizes of 20 nm separated by 40 nm, (b) templated pattern in SiO_2, and (c) deposition and etching of Si leaves the templated nanocrystals in SiO_2 matrix, and (d) spread in the initial copolymer pattern dimensions (dotted curve) and final nanocrystal dimensions (solid curve).

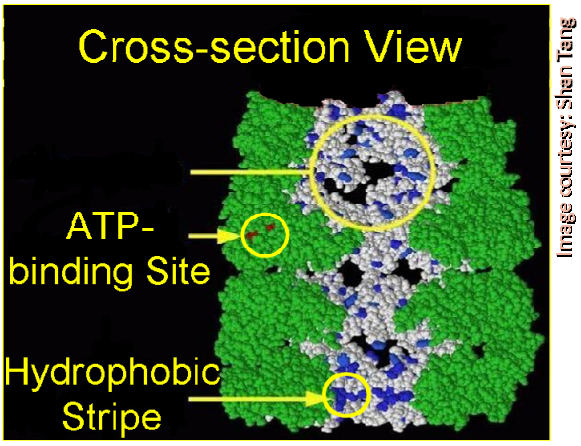
assembly efforts have been focused on Flash memory applications, which requires the assembly process to occur on a SiO_2 (or a high-K dielectric) surface, and must be benign and amenable to silicon-based semiconductor processing. In this regard, Yamashita *et al*. in particular, have demonstrated artificially bio-mineralized cobalt oxide cores accommodated in "ferritin" protein molecules as floating-gate charge storage nodes, where the medium of ferritin molecules served as both nanocrystal synthesizer and self-assembly template.[43] However, possible drawbacks of that technique can include a restriction in the choice of the nanocrystal material to metals and metallic complexes, and lack of dissociation of the nanocrystal formation and assembly processes which can otherwise allow independent fine-tuning of the size and ordering of nanocrystals. Thus, an effort was initiated by Tang *et al*. to exploit properties of the Chaperonin 60 or GroEL protein molecules to mediate and template the ordering of preformed nanocrystals as floating-gate of a Flash memory cell.[44]

Tang *et al.* demonstrated that a commercially available colloidal suspension of preformed semiconductor and metallic nanocrystals can be made to assemble in an ordered two-dimensional array on the surface of dielectric (SiO_2 or HfO_2) substrates.[44] This becomes possible by virtue of properties of the Chaperonin 60 protein molecules that are large multimeric structures shaped like doubly stacked donut-rings with a central cavity size of 4.6 nm and wall thickness of 4.5 nm (fig. 3.2). Also, the interior cavity surfaces of these protein molecules are lined with hydrophobic ligands. Chaperonin 60 belongs to the group of "molecular chaperones", which are a class of proteins that help accelerate protein folding in a biological cell. Non-covalent interactions between these protein molecules cause them to self-assemble into an ordered array on a pretreated dielectric surface. On being subsequently treated with nanocrystals suspended in a colloidal solution, hydrophobically-functionalized (i.e. attached to hydrophobic ligands)

nanocrystals are attracted and attached site-specifically to the central cavity of the already self-assembled, ordered GroEL array by hydrophobic-hydrophobic interactions.[45] After a subsequent anneal that oxidizes the carbon and hydrogen atoms making up the protein



(a)



(b)

Figure 3.2: (a) External views, and (b) Cross-sectional view of Chaperonin 60 (GroEL) protein molecule that enables assembly of preformed nanocrystals into an ordered two-dimensional array.[44]

scaffold to carbon dioxide and water-vapor, respectively, an ordered array of nanocrystals is left behind. A schematic representation of the process steps is illustrated in fig. 3.3.

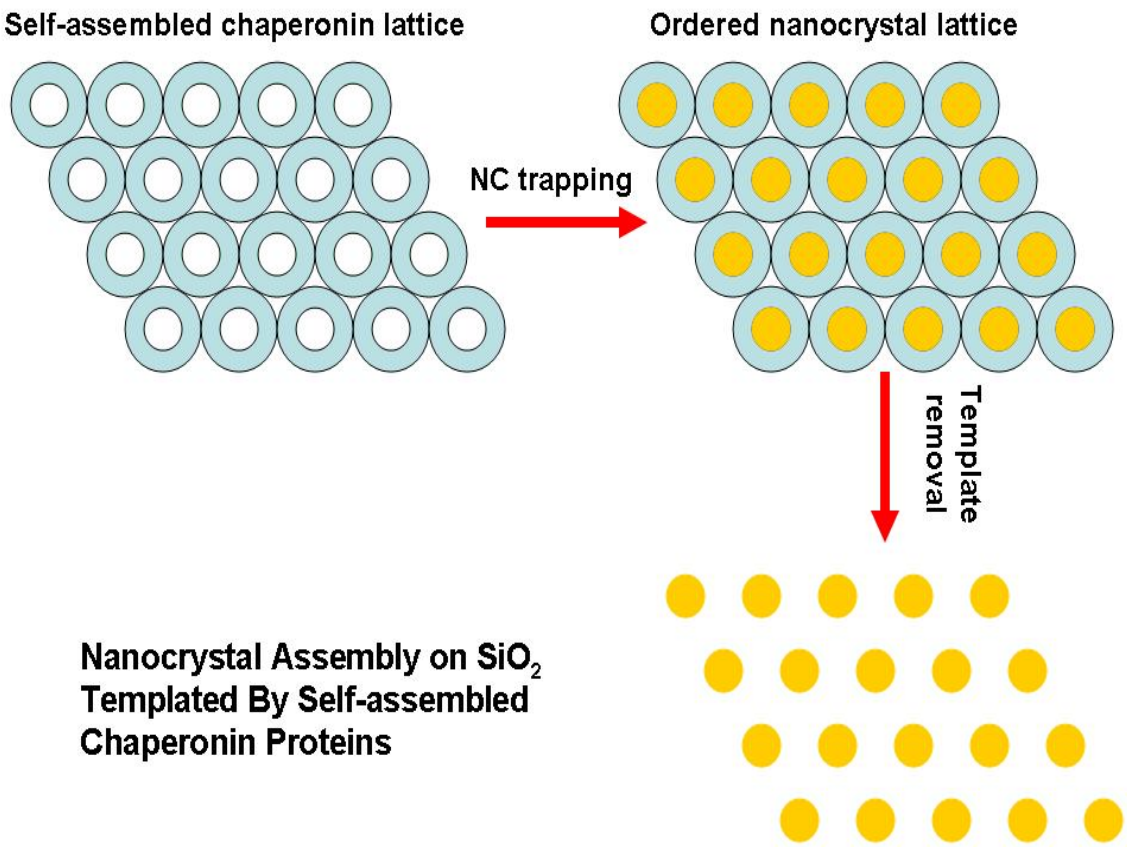


Figure 3.3: Schematic representation of the mechanism for the protein-mediated assembly of nanocrystals (courtesy Shan Tang).

Given the fact that the nanocrystals are preformed and commercially obtained, the aforesaid protein-mediated assembly achieves a complete independence of the parameters critical to good size uniformity and good ordering. In other words, the commercial production process of the nanocrystals account for their size uniformity, while the parameters pertinent to the protein molecules account for the ordering. In the case of

nanocrystals used in the devices described here, the manufacturer[46] supplied the nanocrystals with a reasonably tight distribution uniformity (~ ± 0.5 nm for the 4.5 nm nanocrystals), while the protein molecules are known to be subjected to conformational change altering their cavity size in the presence of Mg^{2+}, K^{+} ions and Adenosine Triphosphate, potentially acting as a size filter.[47] Genetic engineering of the GroEL, and use of other similar protein-molecules is an active domain of biological research, which can enable altering the separation between the individual nanocrystals.[48]

The process steps involved in the protein-mediated assembly are illustrated in fig. 3.4. After the thermal oxidation step to form the tunnel-oxide, the wafer is treated with 5 % Phenyltriethoxysilane (PTS) solution for an hour, when the PTS molecules form a self-assembled monolayer. This pre-treatment of the SiO_2 with PTS solution assists in forming an adhesive layer to subsequently bind and scaffold the protein molecules to the oxide surface by the following mechanism. The silane group (-Si-O-C_2H_5) at one tip of PTS molecules covalently bonds to the SiO_2 surface. On subsequently floating the wafer face down in a 0.1 mg/ml GroEL protein solution for about 10 minutes, the phenyl group at the other end of the PTS molecules attach to bottom central cavity of the protein molecules that are lined with hydrophobic ligands, by hydrophobic-hydrophobic interactions. Thus, the two-dimensional "lattice" of protein molecules is oriented horizontally and attached to the oxide surface. When the wafer is then treated with the colloidal solution of the nanocrystals for about 10 minutes, hydrophobic-hydrophobic interaction between the ligands lining the top surface of the central cavity of the protein molecules attract and trap the nanocrystals that are also covered with hydrophobic ligands. The wafer is then removed from the solution and blow-dried with nitrogren. Finally, the protein template is removed by annealing in an oxygen furnace at 200 °C or on an hotplate in air at 300 °C to oxidize away the protein and leaving behind the ordered

array of nanocrystals on the oxide surface. In this process, the key parameters requiring optimization were the PTS concentration and interaction time and the protein solution concentration and interaction time.[44]

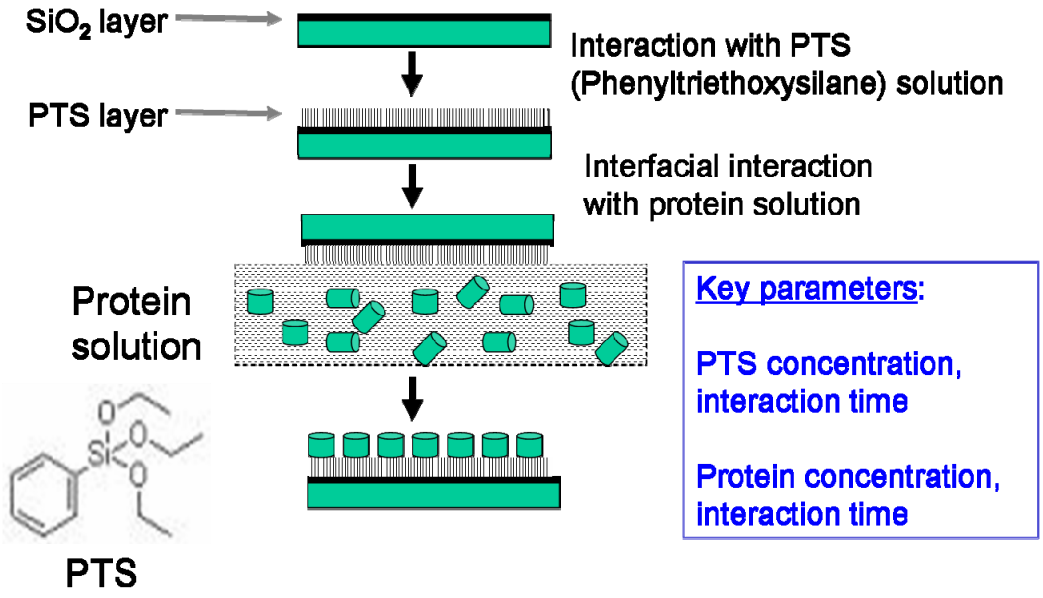
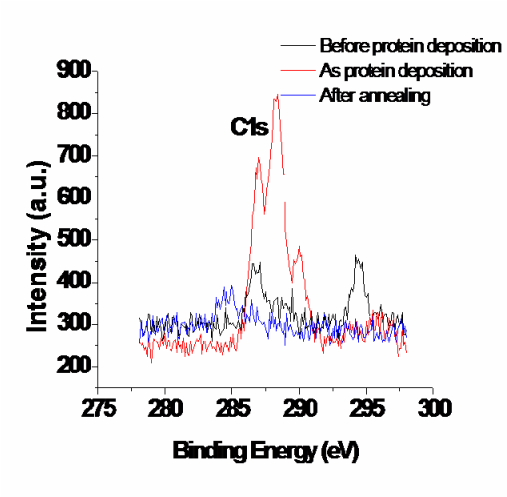


Figure 3.4: Process steps involved in the protein-mediated assembly process.[44]

A legitimate concern against the protein-mediated ordering process is any remnant elements from the protein molecules that may be detrimental to a semiconductor processing environment. However, an X-Ray Photoelectron Spectroscopy scan on the oxide surfaces before, during and after the protein solution treatment of the surface reveals an absence of sodium and carbon atoms after the protein scaffold is oxidized (fig. 3.5).



Element	Area (cts - eV/s)	Sensitivity Factor	Concentration (%)
Si 2p	2774 1724 3056	1.866	82.99 53.83 92.99
C 1s	613 1590 249	2.019	16.96 45.90 7.01
Na 1s	10 49 0	10.263	0.28 0.05 0.00

Figure 3.5: X-ray Photoelectron Spectroscopy elemental scan and signal counts before (in black) and after protein deposition (in red), and finally after protein removal by annealing (in blue), showing lack of remnant sodium and carbon from the protein layer (courtesy Shan Tang).

Physical characterization of the assembled nanocrystals on the oxide surface was performed by Scanning Electron Microscopy (SEM), Transmission Electron Microscopy (TEM) and Scanning Transmission Electron Microscopy (STEM), revealing a significantly ordered assembly process (fig. 3.6).[42, 44] The assembly process has been found to be continuous over areas of the order of 1 μm^2 with work in progress to span the process over larger areas.

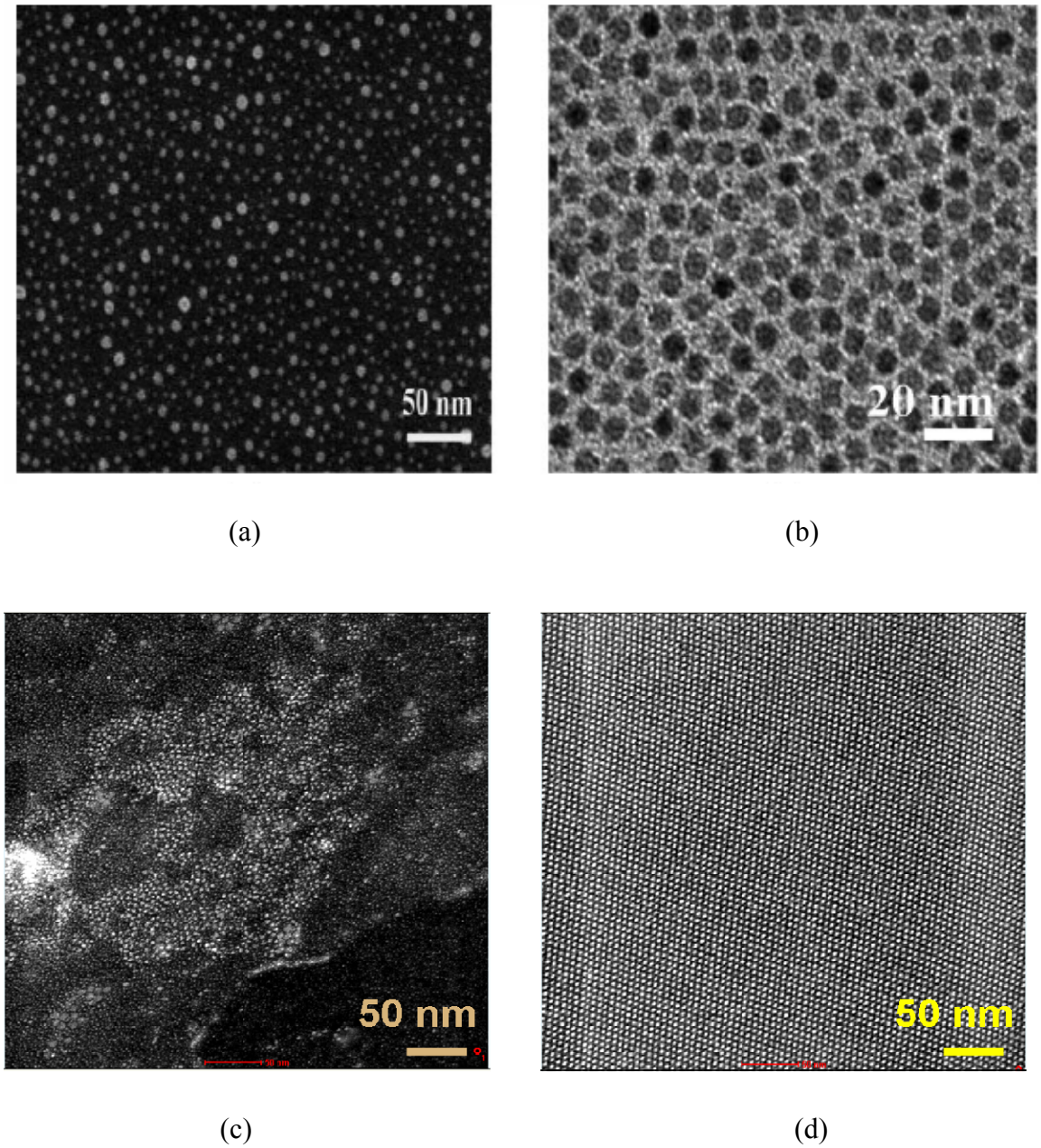


Figure 3.6: Characterization of the protein-mediated ordering of nanocrystals on planar SiO_2 surface. (a) Scanning Electron Micrograph of PbSe nanocrystals after the protein scaffold has been removed by annealing, (b) Transmission Electron Micrograph of ordered Co nanocrystals, and Scanning Transmission Electron Micrograph of PbSe nanocrystals (c) without and (d) with protein-mediated assembly, revealing the efficacy of the ordering process (courtesy Shan Tang).

While the protein-mediated assembly process developed by Tang *et al.* had been shown to work on planar surfaces and transistors, the mechanics of the process are known to be independent of gravity. Therefore, application of the protein-mediated assembly of nanocrystals on the vertical sidewalls for optimum scalability and manufacturability of the vertical Flash transistor is described in the following sections.

3.1.2 Vertical Flash transistor with protein-mediated assembly of nanocrystal floating-gate

The processing of the vertical Flash transistor was optimized and simplified based on the learning developed from the devices described in chapter 2. First, the implantation of the source/drain regions and the sidewall polysilicon was unified as one single step after gate-stack formation, which in turn eliminated the nitride deposition step. Second, the unified implantation step was optimized by the use of three-dimensional Synopsys™ Taurus® process simulation tools for improved transistor electrical characteristics. Thus, implantation at 15 ° tilt with a higher energy of 30 keV was found to sufficiently dope a 100 nm-thick sidewall polysilicon gate as well as the drain/source regions at the base and top of the mesa, compared to separate steps for the gate and source/drain described in chapter 2 (the simulations generally indicated that the tilt angle necessary is a function of the mesa height and area). The corresponding dopant activation was also a single step of Rapid Thermal Anneal at 800 °C for 1 minute. With these process modifications, since the source/drain implantation and activation occurred after the entire gate-stack deposition, better control became achievable over source/drain dopant diffusion regions determining the junction resistance and channel length of the vertical transistor. Also, Boron-doped Si wafers with a heavier doping of 1 x 10^{17} cm^{-3} was used for longer

channel lengths (by virtue of having reduced junction depths) compared to devices described in chapter 2. The modified processing is schematically illustrated in fig. 3.7.

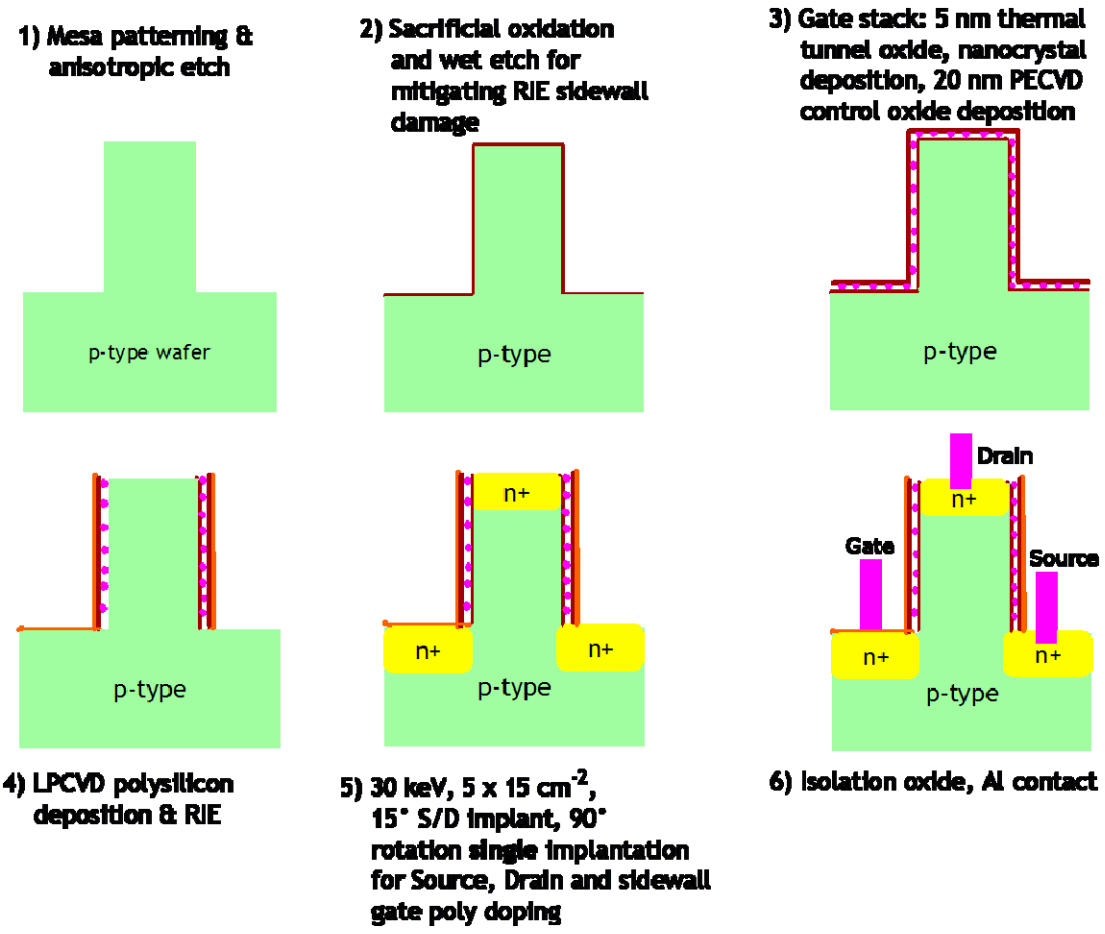
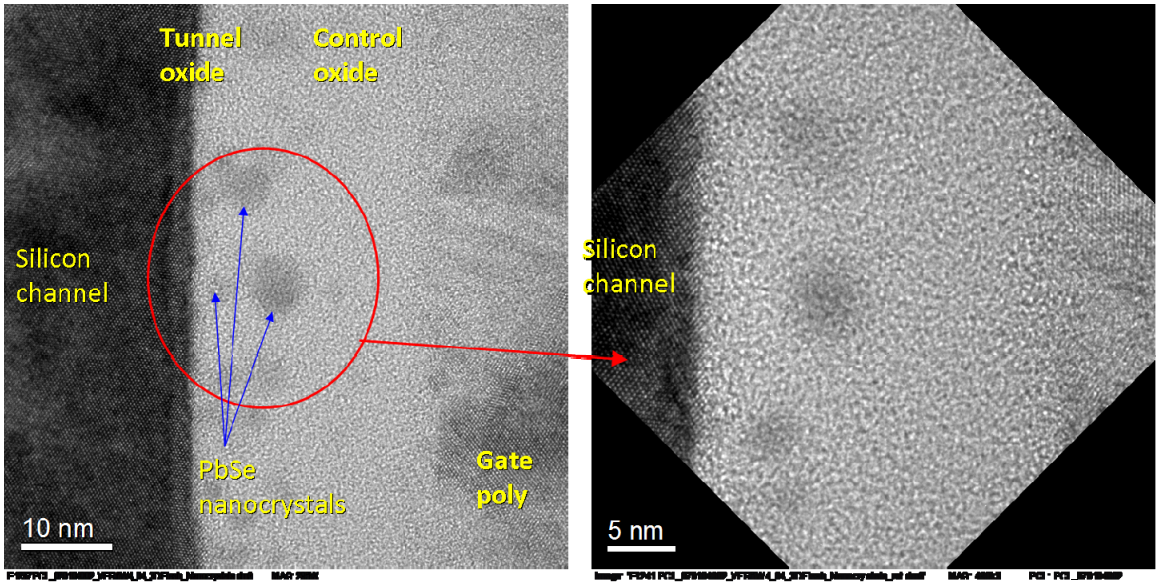


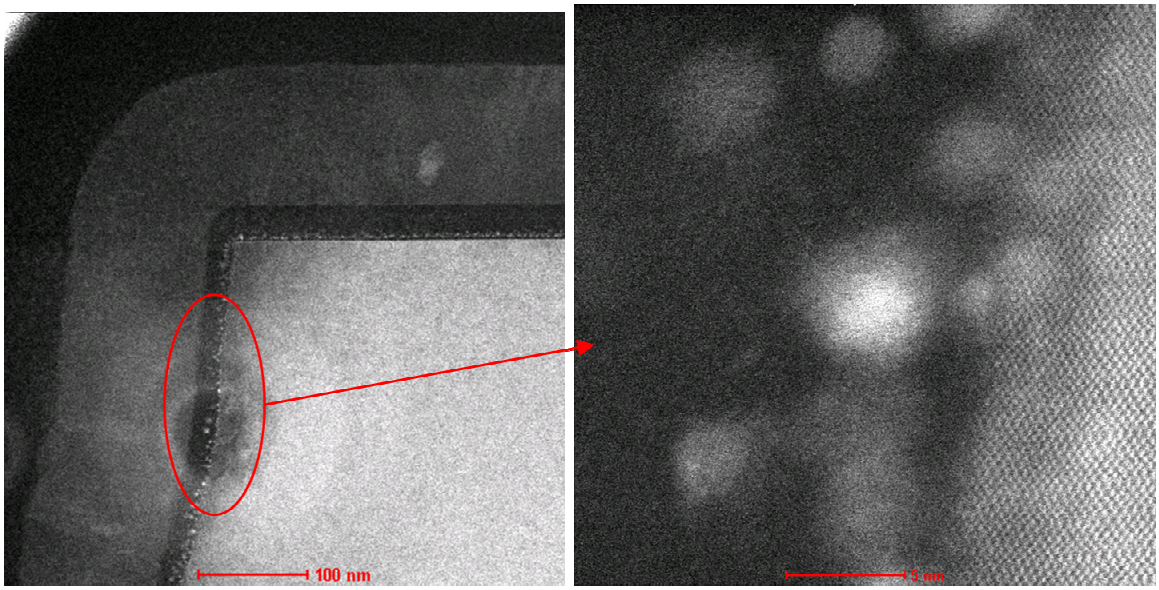
Figure 3.7: Simplified and optimized process-flow for the vertical transistor yielding improved transistor characteristics.

The protein-mediated assembly process for the vertical devices was carried out identically to that for the planar surface (section 3.1.1) with 5 nm and 8 nm PbSe nanocrystals (all reported data pertain to 5 nm nanocrystals). However, the scanning-electron and scanning-probe based physical characterization methods were either impossible or unsuccessful in the case of the vertical sidewalls. Thus, cross-sectional

Transmission Electron Microscopy was deemed to be the only reasonable means of assessing the protein-mediated assembly process in the vertical devices. This intricate characterization was carried out in collaboration with the Advanced Technology Development Facility at the International Sematech. Figure 3.8 shows the cross-sectional High-Resolution Transmission Electron Micrographs of a thin slice of the vertical mesa milled out for analysis. In these micrographs, the discrete nanocrystals are most likely visible from multiple vertical planes, and bending of those planes at the microscopic level from Reactive Ion Etching is a likely reason for the various nanocrystals from those planes appearing to differ in their positions (and corresponding contrast) against the backdrop of the gate-stack oxide matrix. However, the evident discreteness of the sufficiently isolated nanocrystals does indicate the efficacy of the assembly process on the vertical sidewalls. The Dark-Field Transmission Electron Micrograph further clarifies a successful deposition and ordering of the PbSe nanocrystals on the vertical sidewalls.



(a)



(b)

Figure 3.8: (a) Cross-sectional High-Resolution Transmission Electron Micrograph of a thin slice of the vertical Flash transistor to reveal PbSe nanocrystals embedded in the gate-stack and, (b) Half-Angular Dark Field cross-sectional Transmission Electron Micrograph further illustrates the assembly of the nanocrystals on the vertical sidewalls (courtesy Domingo Garcia, ATDF, Sematech).

PbSe nanocrystals with diameters of 5 nm (and 8 nm) were chosen for the vertical transistors because they had been found to produce favorable memory characteristics for planar capacitor structures.[44] With an electron affinity of 4.2 eV similar to Si (fig. 3.9), PbSe provides a sufficiently deep conduction-band potential-well for storing electrons, necessary for good retention characteristics. For planar capacitor structures, other semiconductors (such as SiC [49]) and metals (such as Co and Ni) had been found to work as well, although metal nanocrystals had been usually found to be somewhat incompatible with the thermal budget of a full transistor process flow.[42, 44]

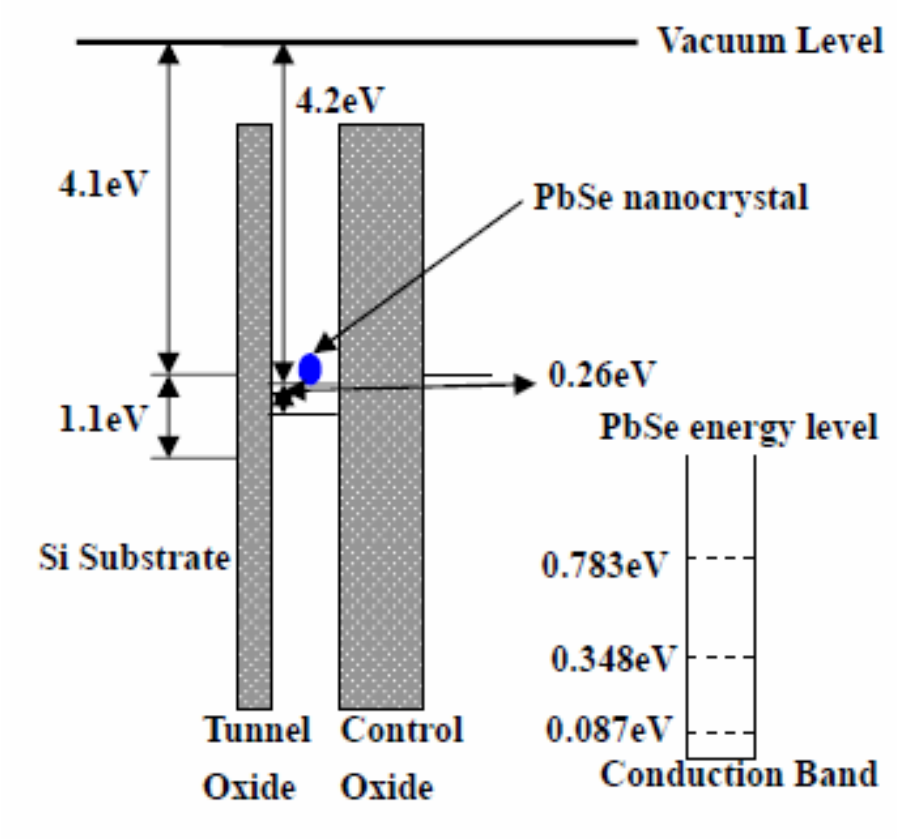


Figure 3.9: Band diagram and occupational energy levels of PbSe nanocrystal floating-gate embedded in the gate-stack.[44]

3.2 Electrical Characterization

The transistor electrical characterization revealed an improved transconductance characteristic (fig. 3.10). First, the sub-threshold swing improved to 110 mV/decade compared to the greater than 160 mV/decade for the transistors described in chapter 2. This improvement can be attributed to the higher body/channel doping levels as well as improved polysilicon implantation step that expectedly resulted in more uniform sidewall doping. It is likely that the transistors described in chapter 2 were affected by the "poly-depletion effect" because of a non-optimized implantation process. Second, the I_{on}/I_{off} ratio of these transistors improved by two orders of magnitude to 10^6, as compared to 10^4 in the case of transistors described in chapter 2, almost entirely from a reduction in the I_{off} value. The latter can be attributed to reduced junction leakage, poly-depletion and short-channel effects resulting from the higher channel/body doping and improved sidewall implantation step of the optimized process. The output characteristics of the transistor are shown in fig. 3.11.

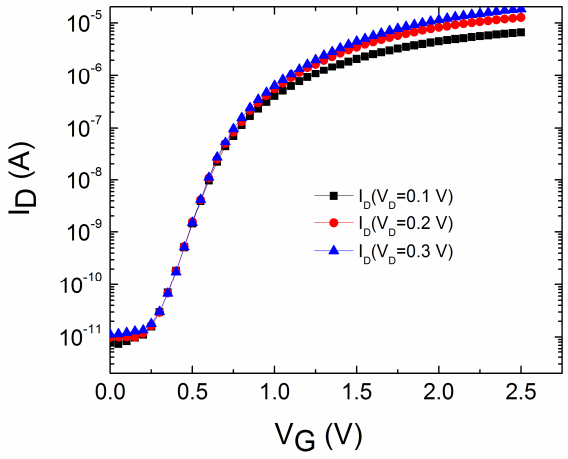


Figure 3.10: Transconductance characteristics of transistors fabricated for protein-mediated assembly of nanocrystal floating-gate (mesa height = 0.9 µm, width = 50 µm, T_{Tox} = 5 nm, T_{Cox} = 20 nm).

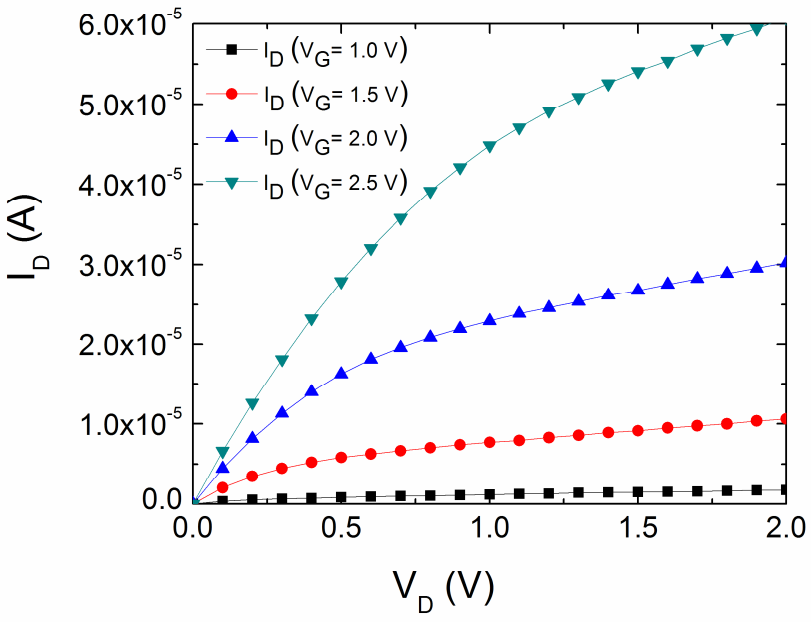


Figure 3.11: Output characteristics of transistors fabricated by protein-mediated assembly of nanocrystal floating-gate (mesa height = 0.9 µm, width = 50 µm, T_{Tox} = 5 nm, T_{Cox} = 20 nm).

The memory performance of the Flash cells were tested with ± 9 V, 100 ms Fowler-Nordheim Tunneling pulses to reveal a maximum memory-window (threshold shift) of 0.5 V (fig. 3.12). Control devices without a nanocrystal floating-gate did not produce a memory window under identical programming conditions evidencing charge-storage within the nanocrystals. On plugging 0.5 V threshold shift in the traditional equation for nanocrystal Flash memory[50],

$$\Delta V_T = \frac{qn_{nc}x}{\varepsilon_{ox}}[t_{control} + 0.5\frac{\varepsilon_{ox}t_{nc}}{\varepsilon_{nc}}]$$

where n_{nc} is the number density of nanocrystals (10^{12} cm^{-2}), t denotes the thickness (diameter) of control-oxide (nanocrystals), ε denotes the dielectric constants, and q the electronic charge, the fractional charge per nanocrystal x is found to be 0.54. This indicates the possibility that optimization of the gate-stack dielectric layers can yield a larger memory window with at least one electron per nanocrystal. Since it is known that poor quality of the control oxide led to charge-trapping and device breakdown (section 2.2), replacing the gate-stack SiO_2 with high-K dielectrics is a possible pathway to optimize the gate-stack, while availing of lower power and/or faster program/erase processes.

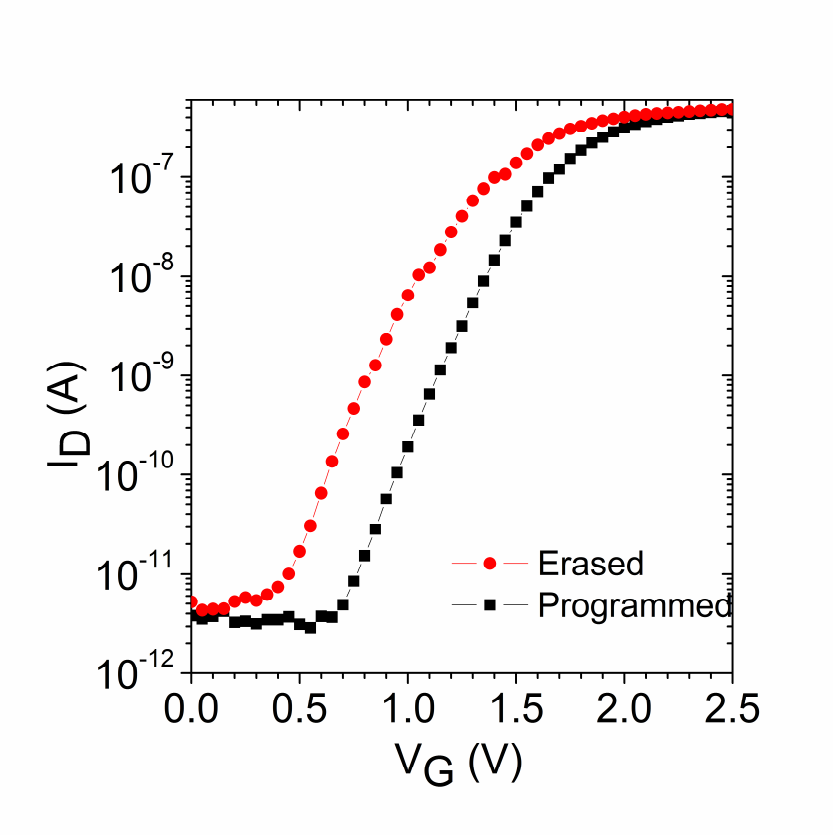


Figure 3.12: Memory window produced by ± 9 V, 100 ms tunneling pulses on PbSe nanocrystal floating-gate Flash transistors.

The retention characteristics measured at room temperature is shown in fig. 3.13, demonstrating a robust memory window typical of nanocrystal memory cells. For these devices however, a high temperature retention measurement could not be performed successfully due to frequent breakdown of the transistors when programmed/erased at 85 °C, caused most likely by increased charge-transport in the SiO_2 control-oxide at high temperature. However, it is worth noting that Tang *et al.* have demonstrated planar devices with similar protein-mediated PbSe nanocrystals to produce good high-temperature retention characteristics[51], implying a necessity for optimization of the gate-stack dielectric quality for improvement of the operational characteristics.

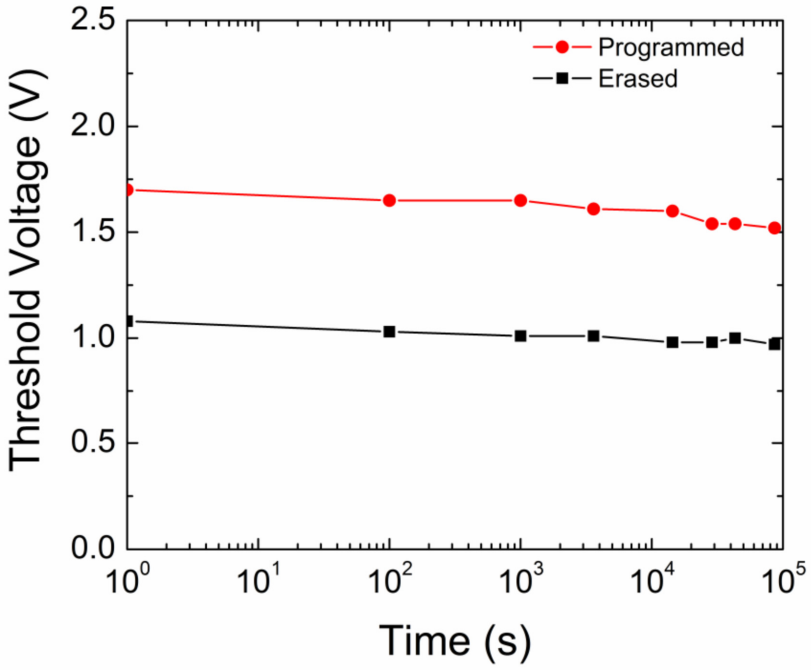


Figure 3.13: Retention characteristics of PbSe nanocrystal floating-gate memory cells at room temperature, initially programmed/erased by tunneling with ± 9V, 100 ms gate pulses.

The endurance characteristics of the memory devices are shown in fig. 3.14. The devices were not programmed to their widest possible memory window to prevent degradation and early breakdown. Thus, with a memory window of about 0.25 V the devices survived 10^5 cycles.

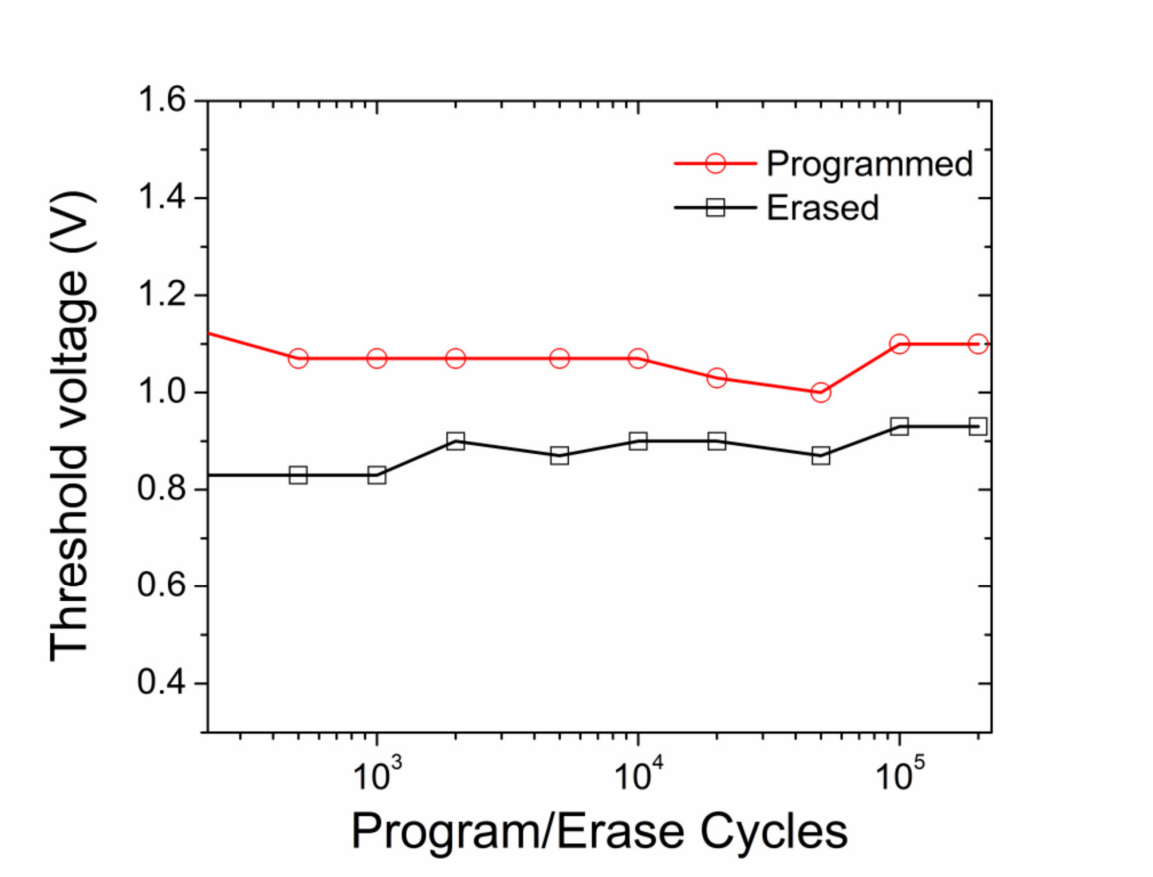
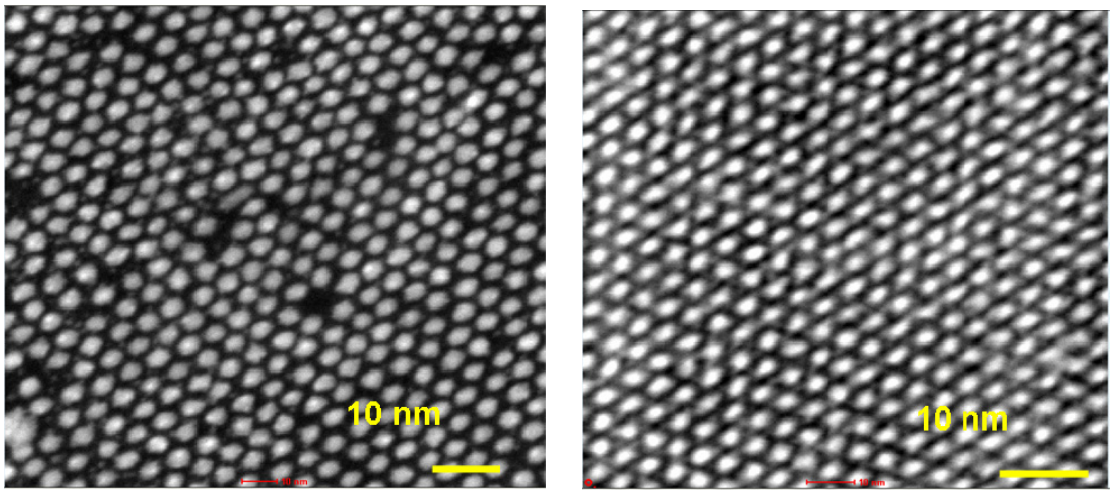


Figure 3.14: Endurance characteristics of PbSe nanocrystal floating-gate memory cells, programmed/erased by tunneling with ± 9V, 100 ms gate pulses.

As previously noted, even though protein-mediated assembly of nanocrystals with diameters of 5 nm as well as 8 nm were used for the vertical devices, memory operation (threshold shift) was observed only for devices with 5 nm diameter nanocrystals. In case of assembly on planar surfaces, it has been observed by Tang *et al.* that assembly of

nanocrystals with diameters closest to the protein-cavity diameter (i.e. ~ 4.6 nm) are nearly defect-free, without noticeable gaps or voids. However, there is significant distortion of the ordering process, including voids, in the case of larger nanocrystals. Figure 3.14 shows a comparison between assembly of nanocrystals with different sizes, where a more favorable assembly process is evident for the 4 nm nanocrystals. In the case of the vertical devices, the lack of memory window for the larger 8 nm nanocrystals can be explained by a lack of significant assembly on the vertical sidewalls, based on the evidently degraded assembly process for larger nanocrystal size. It is conceivable that the larger and bulkier 8 nm nanocrystals were not efficiently captured by the hydrophobic-



(a) (b)

Figure 3.14: Comparison by Scanning Tunneling Electron Micrography, of the protein-mediated assembly processes for (a) 6 nm and, (b) 4 nm diameter nanocrystals on planar surfaces. Nanocrystals with diameter closer to the protein-cavity size (~ 4.6 nm) are evidently better assembled by the protein molecules.[51]

hydrophobic interactions with the protein-cavities when in competition with gravitational forces, especially considering the comparatively limited contact surface between the

protein-cavities and the larger nanocrystals. Further, the weak Van der Waals forces likely responsible for attaching the nanocrystals to the vertical sidewalls could also possibly be less effective for the bulkier nanocrystals. While a repetition of this experiment and more extensive physical characterization could confirm this hypothesis, this observation still provides an indirect evidence of the efficacy of the assembly process on vertical sidewalls.

In summary, the protein-mediated assembly of preformed nanocrystals was applied to the vertical Flash memory cell and characterized physically and electrically. The protein-mediated assembly process that had been developed for planar surfaces and devices was found to work on the vertical sidewall surfaces without any modification. Implemented process improvements yielded improved electrical performance of the vertical Flash transistor described in this chapter. While there is further room for improvement in the gate-stack dielectrics, especially with regards to their quality that can allow thinner layers, use of high-K dielectrics was identified as a means of augmenting the figures of merit of the devices. Specifically, while retaining SiO_2 as the tunnel oxide for optimum compatibility for the protein-mediated assembly process, aluminum oxide (Al_2O_3) could be a viable choice for the control-oxide since it has similar conduction band-offset as SiO_2 (fig. 3.15), therefore aiding with retention and programming with limited tunneling current to the gate electrode. Recent reports have also indicated interest in the use of Al_2O_3 as the control-oxide dielectric in Flash memory cells and arrays.[53]

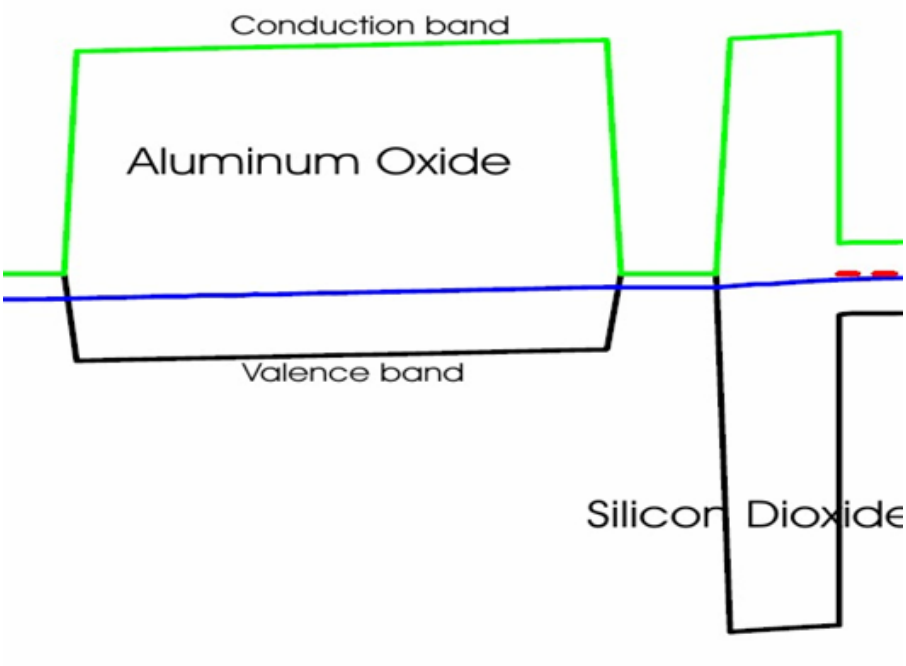


Figure 3.15: Band-diagram of gate-stack layers with aluminum oxide as control-oxide and retaining SiO_2 as the tunnel-oxide would offer similarity of the conduction-band offsets while not disturbing the protein-mediated assembly process on the tunnel-oxide.

Part II: Phase Change Memory as an alternative technology to replace Flash

CHAPTER 4

Improvement of Phase Change Memory with Operating Cycles

In the continued quest for enhancing the density and cost-per-bit of mainstream non-volatile memory technology enabled by long-term scaling prospects, as well as for improving on the key performance metrics of Flash memory, research and development on Phase Change Memory has recently revealed compelling arguments in its favor for ultimately replacing floating-gate Flash technology.[23] While phase change materials such as the Germanium Antimony Telluride ($Ge_2Sb_2Te_5$, or GST) alloy have been thoroughly investigated for their application in rewritable CD and DVD optical storage media,[54] electrical operation of Phase Change Memory cells have revealed additional phenomenon necessitating renewed investigations. Since the fundamental operation of Phase Change Memory is based on the non-destructive physical process of phase-transformation between amorphous and crystalline states, Phase Change Memory offers the *theoretical* possibility of unlimited cycles of operation. In this chapter, after discussing relevant materials properties and physics, a fundamental understanding of an aspect of phase change technology is attempted by studying the effect of operational cycles on its key figures of merit, viz. reset and set-state resistances and threshold voltage.

4.1 Material, Technology and Physics of Phase Change Memory

4.1.1 Germanium Antimony Telluride ($Ge_2Sb_2Te_5$) as memory material

Central to the operation of a fundamental PCM cell is the volume of "chalcogenide" material characterized by the presence of at least a Group VI element ("chalcogens" such as Te) and/or an element from Group V (such as Sb). While many different phase change materials have been described in technical literature (fig. 4.1), "congruent" crystallization in $Ge_xSb_yTe_z$ (GST) alloys involving a *rapid and reversible* transformation between the disordered, amorphous state and ordered, crystalline state is exploited in rewritable optical media and the PCM cell. In the case of GST, the rapid and reversible crystallization process based on "threshold switching" can be made to occur

Binary	Ternary	Quaternary
Ga Sb	$Ge_2Sb_2Te_5$	Ag In Sb Te
In Sb	In Sb Te	(Ge Sn)Sb Te
In Se	Ga Se Te	Ge Sb (Se Te)
$Sb_2 Te_3$	Sn Sb_2 Te_4	$Te_{81}Ge_{15}Sb_2S_2$
Ge Te	In Sb Ge	$Ge_2Sb_2Te_5$:N
Si_xSb_{100-x}	$Si_2Sb_2Te_5$	$Ge_2Sb_2Te_5$:O
$Sb_{65}Se_{35}$		$Ge_2Sb_2Te_5$Sn
		$Ge_2Sb_2Te_5$Bi

Figure 4.1: Various phase-change alloys described in literature. While many are used in "write-once" optical media (CD-R, DVD±R), some like $Ge_2Sb_2Te_5$ are more suitable for rewritable media (DVD-RAM) and the PCM cell for their fast switching characteristics.[55]

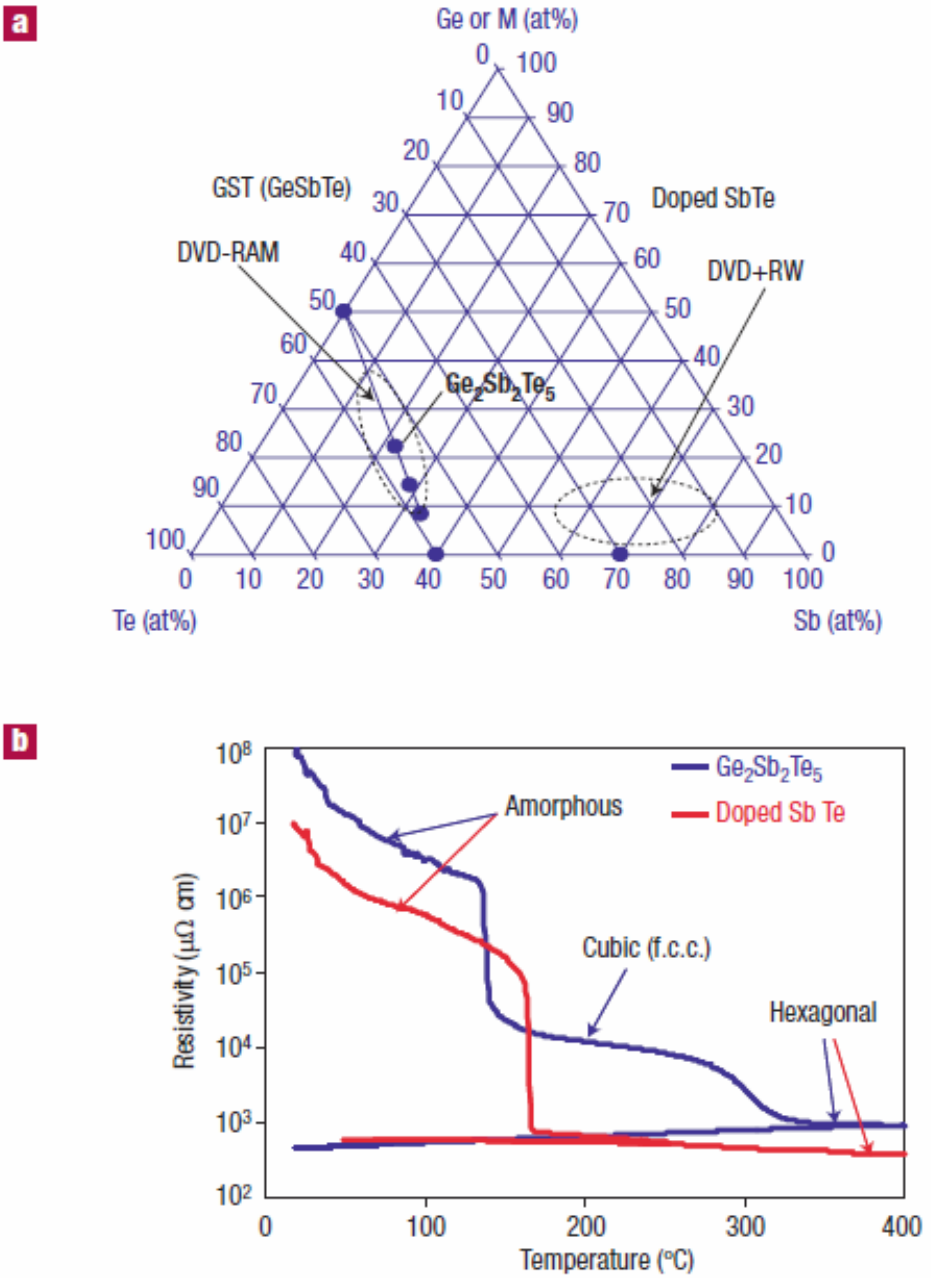


Figure 4.2: (a) Phase-diagram of the Germanium-Antimony-Tellurium alloy system with pseudobinary line of compositions for GST that show rapid, reversible crystallization conducive to DVD-RAM and PCM. (b) Resistivity vs. temperature characteristics of chalcogenide alloys.[56]

for GST compositions along the pseudo-binary line shown in fig. 4.2 (a). The crystalline state of the chalcogenide, otherwise known as the "SET" state, is the thermally stable one, as opposed to the amorphous or "RESET" state that transforms to crystalline state on annealing. The activation energy of transformation from amorphous to crystalline states and the speed of crystallization are competing requirements on any of these material systems chosen for the memory application. Hence, for optical media targeted at "write-few, read-many" applications and long shelf-life, Sb-Te alloys doped with Ge, In, Ag and Ga are usually favored for their very high activation energy of crystallization. On the other hand, for the PCM cell and DVD-RAM media requiring optimally fast switching with good retention, $Ge_2Sb_2Te_5$ is usually the material system of choice (fig. 4.3).

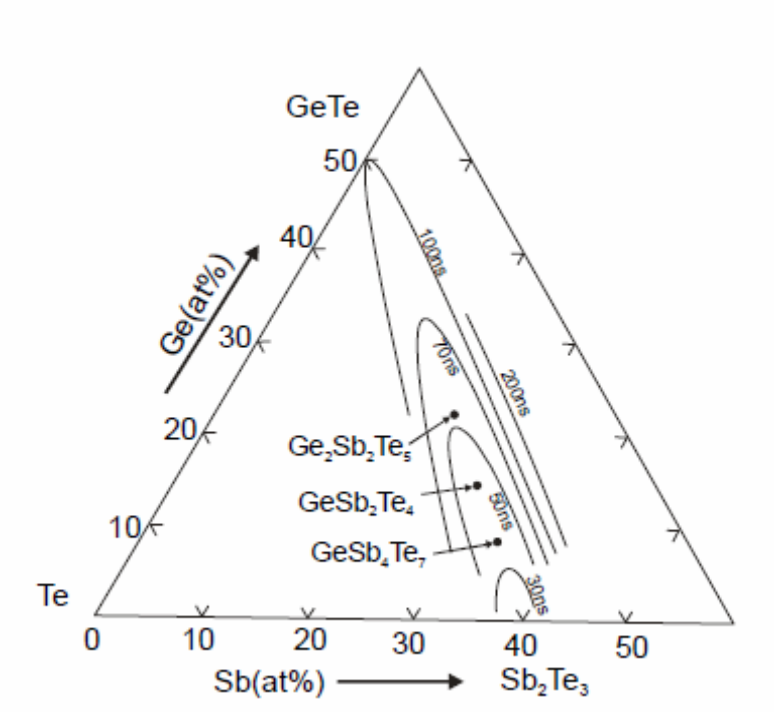
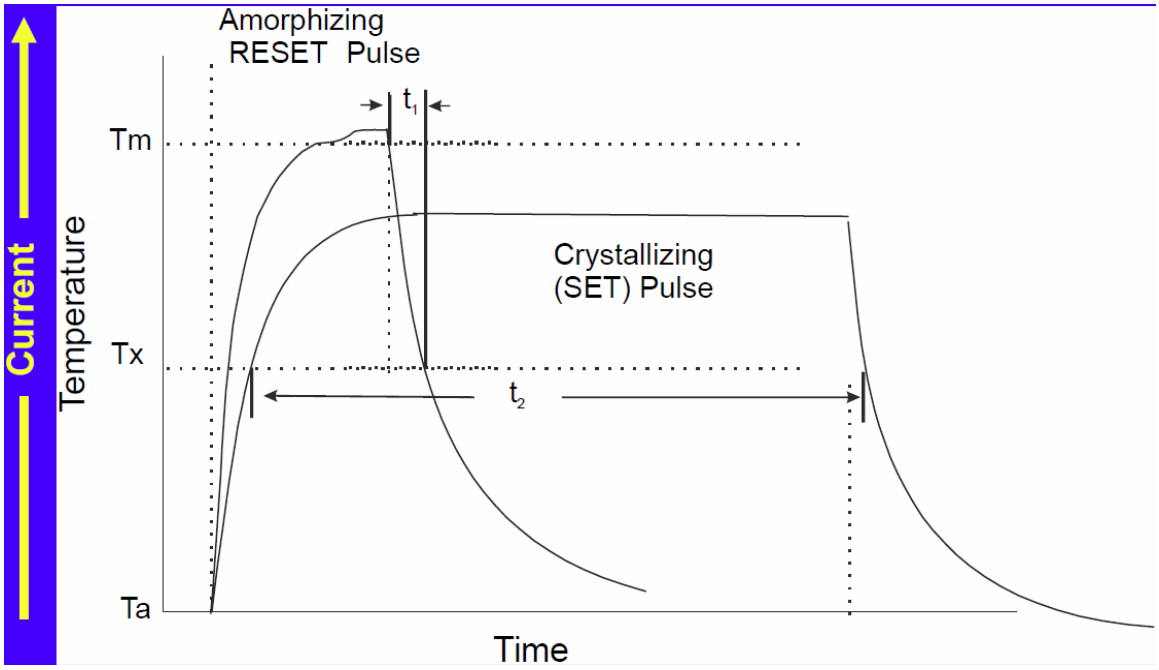


Figure 4.3: Compositional dependence of laser-induced crystallization speed in GST alloy films on GeTe – Sb_2Te_3 pseudo-binary tie-line.[56, 58]

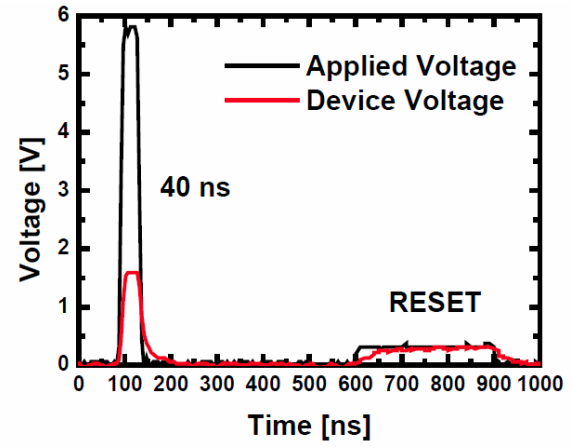
4.1.2 Phase Change Memory cell structure and basic operations

The basic structure of the PCM cell typically consists of a thin film of GST material deposited on the top of a heater electrode made of titanium (Ti/TiN) as shown in fig. 4.5a. The contact area of the heater with the GST film is critical in determining the "programming current", which is the current necessary to melt the GST by Joule heating. Due to the processing thermal budget involved after the GST deposition, the GST film immediately after the wafer processing is in the thermally stable crystalline state. Thereafter, only a small volume of the GST above the contact area, often called the "active volume", actually toggles between crystalline and amorphous states dependent on the applied pulse current and width. Figure 4.4a shows the RESET/amorphizing and SET/crystallizing pulse shapes. A RESET programming pulse with sufficiently large amplitude but short width raises the temperature of the GST active volume above its melting point of ~ 620 °C and subsequent rapid quenching results in an amorphous/RESET state of the active volume. On the other hand, a SET programming pulse with relatively smaller amplitude but longer width heats the active volume above the crystallization temperature while keeping it below the melting point, and the consequent annealing leads to a crystalline state of the active volume. For reading the state of the cell, a pulse with very low amplitude and short width polls the cell resistance without disturbing its material state, as shown in figs. 4.4b and c.

Since the programming current is a key parameter affecting the scalability and reliability of the PCM cell, various novel schemes have been devised to minimize it. The "μ-trench" PCM cell (fig. 4.5b) that the studies described in this dissertation work are based on, has been designed to minimize the physical contact area between the GST and the heater to reduce the active volume, in turn reducing the required programming



(a)



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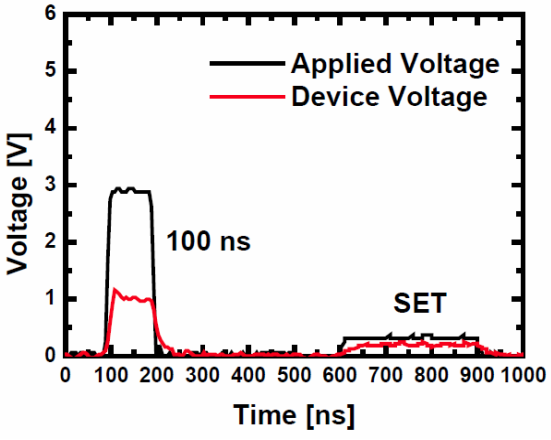
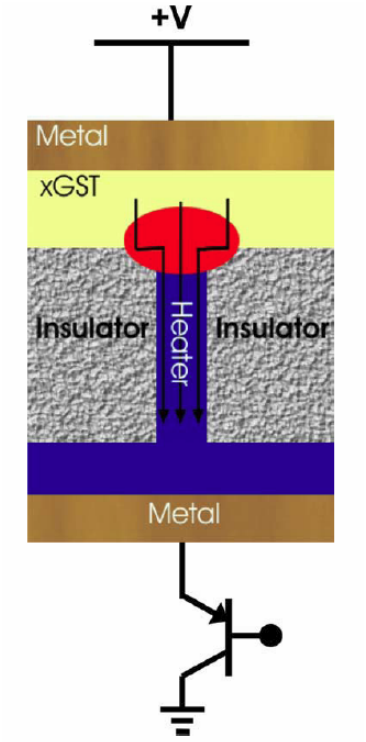


(c)

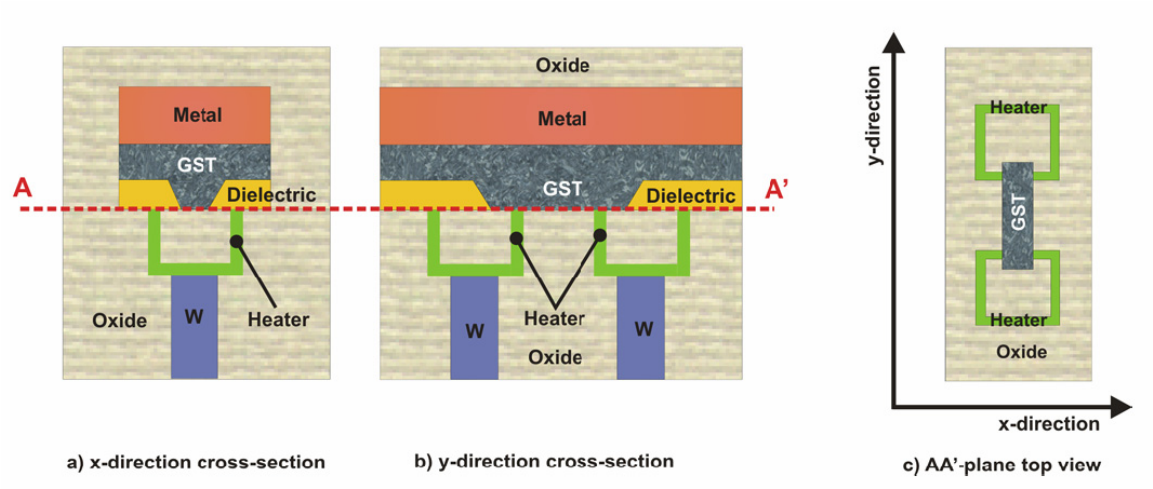
Figure 4.4: (a) Programming pulse characteristics for RESET and SET operations,[25] and (b) & (c) oscilloscope traces of the applied and measured voltages across the device during programming and read-out operations, evidencing the much faster operating speed compared to Flash.[59]

current.[19, 59] Also, since the μ-trench width scales with lithography, programming current and power consumption are expected to improve with successive lithographic nodes. The thermal time-constant of the cell also needs to be carefully designed with appropriate passive materials surrounding it, for optimizing the minimum RESET pulse current together with the shortest SET pulse-width necessary.

Since the basic PCM device itself is a resistive element, an associated transistor or diode based switch is necessary for controlling access to the bit. In this particular implementation, the PCM cell is coupled to a vertical *pnp*-Bipolar Junction Transistor (BJT). The base of the *pnp*-BJT constitutes the word-line, the emitter connects to the bottom electrode (heater) of the resistive element through a tungsten plug ("pre-contact") constituting the bit-line, and the collector forms the common ground. Thus the 1T-1R memory cell achieves a fully self-aligned, cross-point architecture between the active area and the emitter and base implant regions, with a cell area of $10 - 12\ F^2$. It is worth noting here that the area of the PCM cell determining maximum possible array density is primarily limited by the selector device, rather than the resistive element itself. Since this implementation of the PCM cell is targeted at NOR applications,[19] the density requirements are significantly lower than that for NAND arrays. Electron micrographs of a fabricated PCM cell and the BJT selector underneath are shown in fig. 4.6.

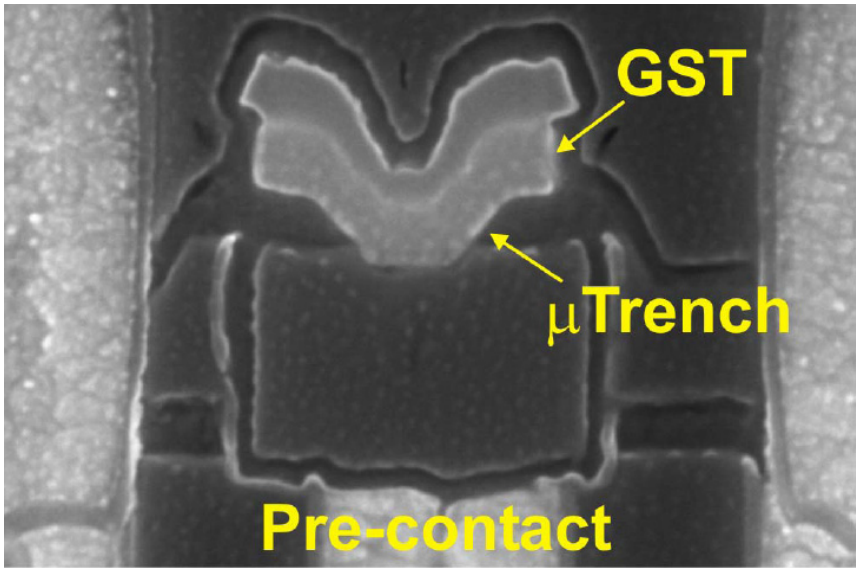


(a)

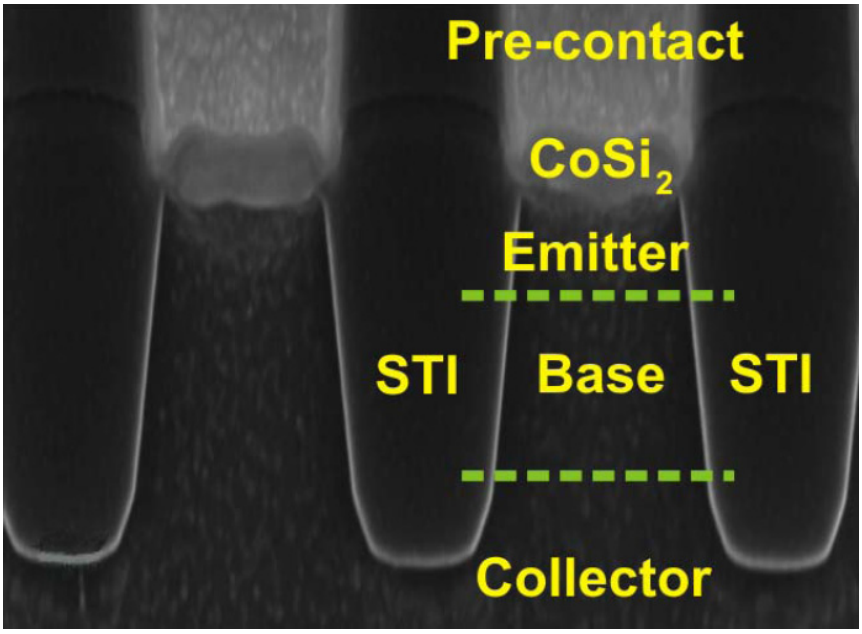


(b)

Figure 4.5: (a) The basic PCM cell [62], and (b) the "μ-trench" implementation by ST Microelectronics for reducing the contact-area and programming current.[19]



(a)



(b)

Figure 4.6: (a) Scanning Electron Micrograph of the μ-trench memory element and (b) the underlying BJT selector device completing the 1T-1R PCM cell (scale not available in published data).[19]

4.1.3 PCM physics and electrical characteristics

The primary figures of merit of the PCM cell are the resistance of the RESET (R_{RESET}) and SET (R_{SET}) states, as well as the threshold voltage (V_{Th}) for switching from RESET to SET state. The cell resistance is fundamentally dependent on electronic transport properties of the amorphous and crystalline states, usually differing by one or more orders of magnitude in a typical PCM cell. While the cell resistance is often a function of the cell design (for instance, contact area of GST and heater), the threshold switching voltage is a more fundamental property of the memory material. Figure 4.7 shows the I-V characteristics of a PCM cell in amorphous and crystalline states, along with the "snapback" associated with threshold switching. When the GST is in crystalline state, the I-V curve is nearly ohmic. With sufficient increase in the bias across the cell so that it reaches the "RESET current regime", local Joule heating at the contact between the GST and the heater causes the GST active volume to melt. If the current pulse is then

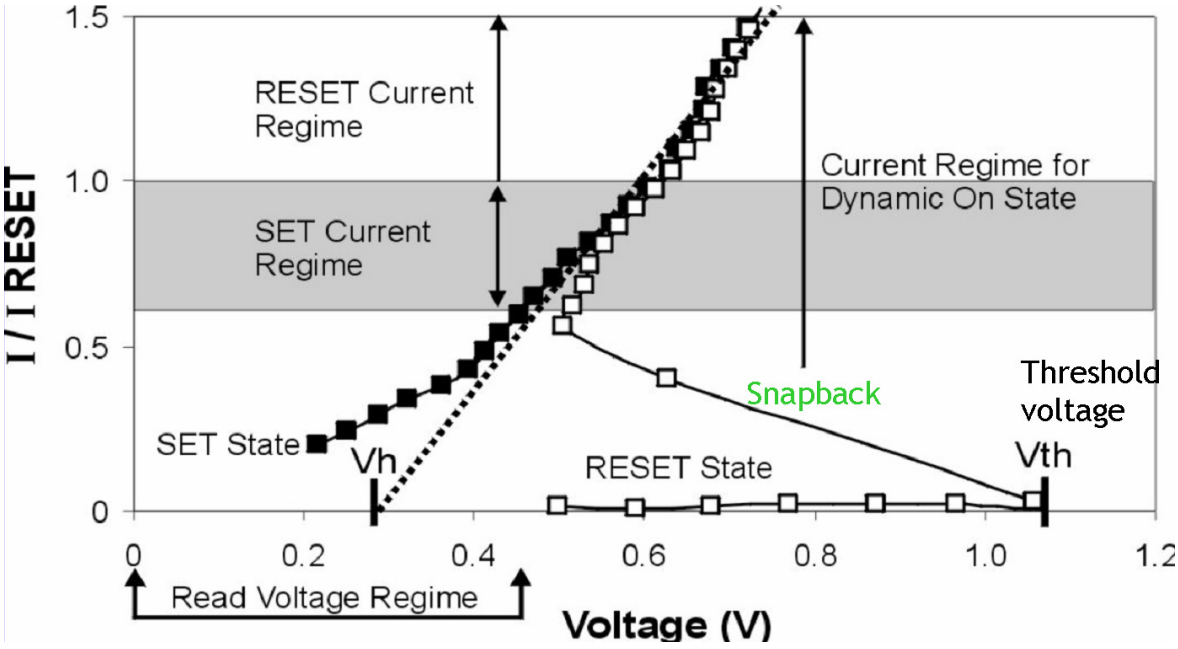


Figure 4.7: I-V and switching characteristics of a PCM cell in its various states.[24]

swiftly quenched, rapid cooling of the molten GST does not leave enough time to rearrange the bonds and therefore ends up in an amorphous state. In the amorphous state, the I-V curve has two distinct regimes of operation. At low biases the resistance is very high, but as the bias is increased above the threshold voltage, Ovonic Threshold Switching (OTS) takes place. OTS is a field assisted, reversible and purely electronic transition that transforms an amorphous semiconductor from a highly resistive to a conductive state. Thus, although the current value swiftly increases with the voltage snapback, the material is still physically in an amorphous state. Further increase in current to the "SET current regime" causes the GST material to anneal by Joule heating, without actually melting it. This latter change in actual physical state of the memory material from amorphous to crystalline is often referred to as Ovonic Memory Switching (OMS) as opposed to OTS.

The theoretical understanding behind OTS is generally somewhat divided between two models, one being thermal and the other being electronic. The thermal model is based on the formation of a hot filament in the GST when the potential drop across it exceeds V_{Th}. More recently, however, there has been considerable evidence on OTS being an electronically driven phenomenon. Pirovano *et al.* have proposed that raising the voltage across the amorphous GST material leads to competing electronic generation and recombination processes to occur simultaneously.[60] According to their model, the generation of carriers occurs in chalcogenides by a mechanism that is dictated by the electric field through the material. At every bias point of the I-V characteristics, recombination processes also occur via trapping centers, to the effect that it balances the generation process. However, at high enough current concentrations almost all available traps are filled by the generated carriers so that the recombination current only slowly increases with the bias. Since the generation rate is understood to be exponentially

dependent on the bias, at the critical voltage of V_{Th} across the material, the recombination rate is completely flooded by the generation rate. Thus, the only way to reach a steady state would then be by a reduction in the bias across the material, which is manifested as the snapback phenomenon, consequently reducing the generation rate. However, since the snapback occurs simultaneously with an exponential increase of current, the carrier generation rate must also be dependent on the existing carrier density; the latter thus defraying the effect of exponential potential drop across the GST that leads to the reduced carrier generation rate at snapback. Thus, the carrier generation rate being exponentially dependent on the electric field but also increasing with carrier concentration, Pirovano *et al.* inferred the generation mechanism to be impact ionization. Simulations based on their model showed a slight increase in V_{Th} with temperature, indicative of the trend expected from impact ionization and counter to the trend expected from alternative generation mechanisms such as thermal or Poole-Frenkel thermo-ionization (fig. 4.8).

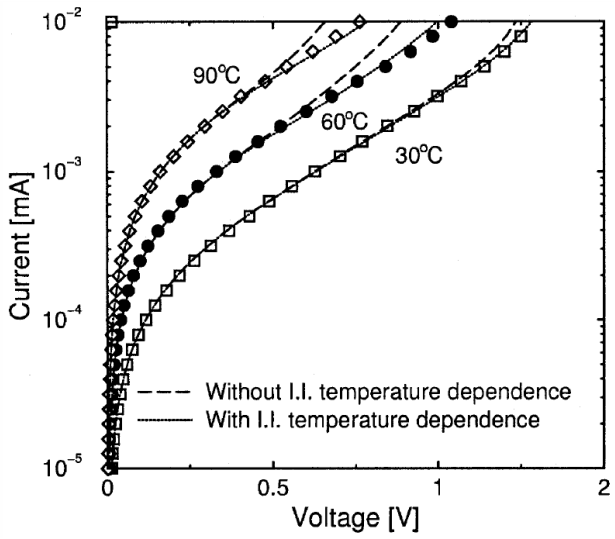


Figure 4.8: Comparison between experimental (symbols) and simulated (lines) I-V curves at different temperatures for amorphous GST resistor. A better agreement between experimental and numerical data is evident when temperature dependence of impact ionization is included in the simulation model.[60]

The nature and compositional phase of the active volume of GST has also been the subject of significant debate in the last few years, on whether there is a series or parallel distribution of the amorphous and crystalline material that determines the resistance and threshold voltage of a given state. As shown in fig. 4.9, in partially-RESET/SET and fully RESET states of the cell, the active volume can be composed of either a stacked (series) or a parallel composition of amorphous and crystalline GST, which would correspond to different electrical behaviors of the cell. In order to probe such electrical behavior of a PCM cell, an "R-I curve" is often useful. Successive programming (RESET) pulses with a fixed, short width but gradually increasing amplitude (i.e. current) on a PCM cell can take it through the entire spectrum of operational states, viz. RESET, SET and partially RESET/SET. The plot of the resistance (R) vs. the programming pulse current (I) of the PCM cell (the "R-I curve") is thus an important characterization and diagnostic tool for probing cell characteristics. Figure 4.9 shows the R-I curves of a cell initially in SET as well as RESET states, going through intermediate states, finally ending in a fully RESET state of the cell. For an initially RESET cell, the gradual increase in Joule heating with increasing programming current

Figure 4.9: Schematic representation of possible phase distribution of material in the active volume of GST for non-SET cells. (a) Fully and (b) partially RESET states with stacked distribution and (c) parallel distribution of phases.[61]

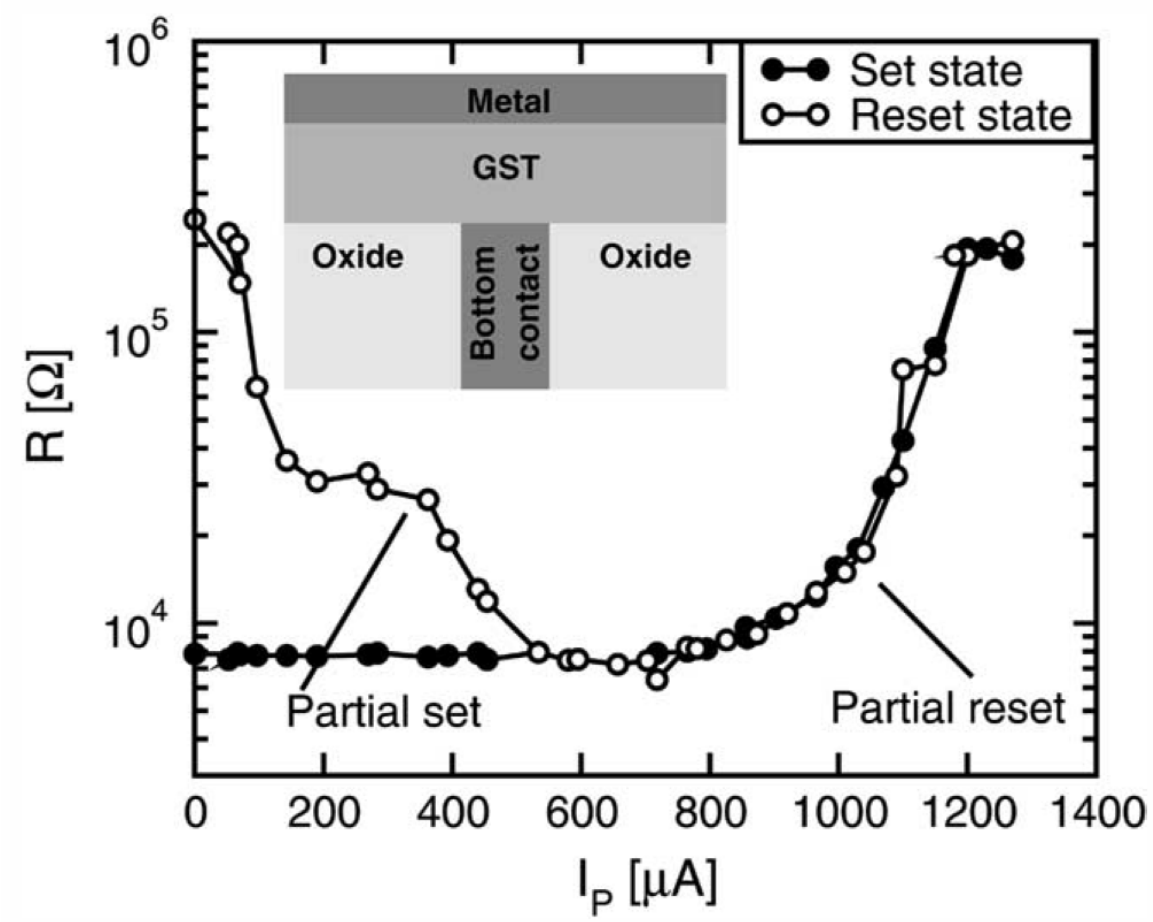


Figure 4.10: Cell resistance vs. programming current (R-I) curves starting from SET as well as RESET conditions.[61]

initially causes crystallization until the GST melting point is reached, when amorphization occurs instead. In the R-I curve shown, the partially RESET and SET states are significant, since they can allow considerable insight on the phase distribution in the GST active volume. This example curve was collected with 100 ns program pulse-widths and 1 μA read current. In this plot, beyond ~ 700 μA of programming current corresponding to the approximately optimum SET state of the bit, points corresponding to the initially RESET state of the bit overlap with those for the initially SET state. This indicates that the partially RESET states lying beyond the optimum SET condition are

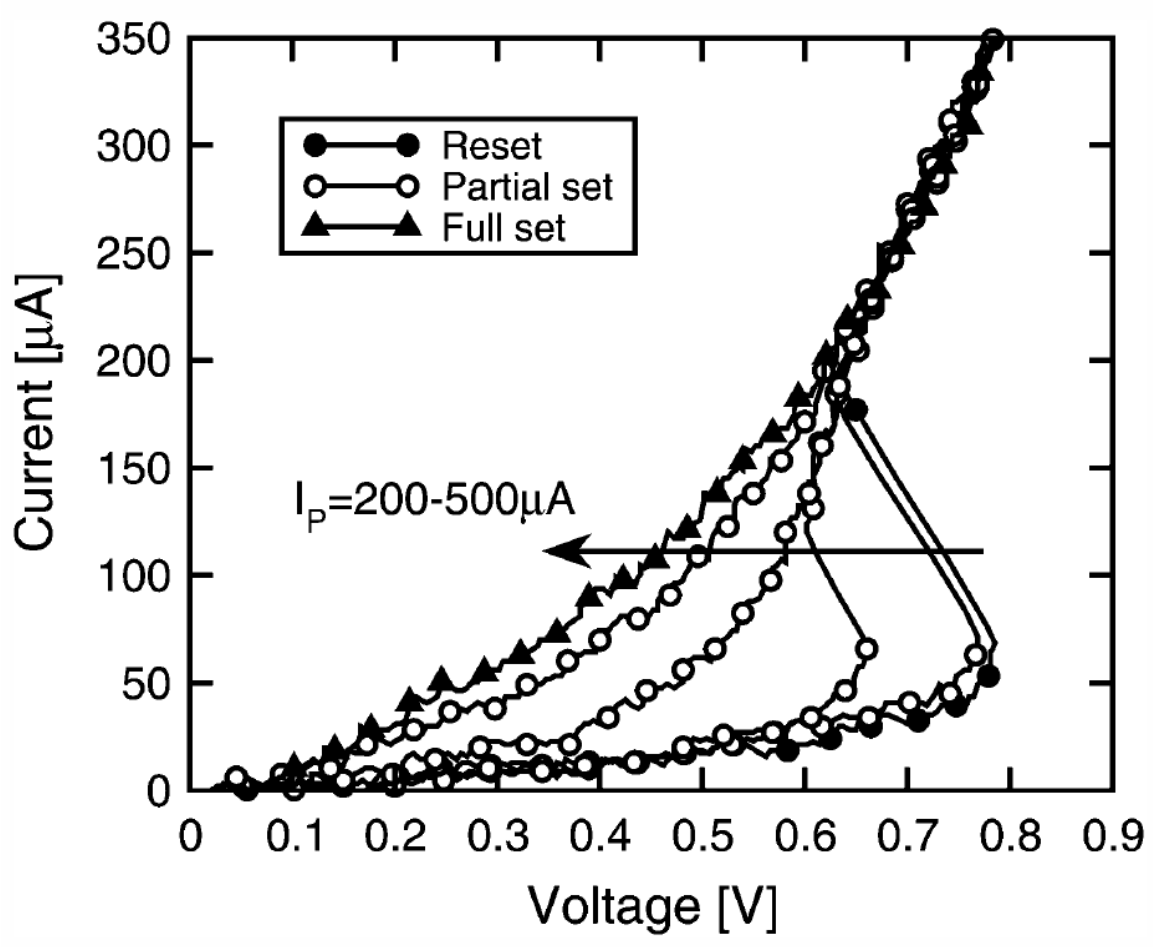


Figure 4.11: I-V curves of fully and partially RESET/SET condition of a cell.[61]

electrically similar irrespective of the different initial state of the bit, and the evolution of the RESET *resistance* occurs gradually, rather than abruptly as OTS. A gradual change in resistance holds true for the transformation from RESET to SET states as well, as evidenced by the R-I curve for the initially RESET state of the bit, even though the abrupt threshold switching accompanies this latter transition. In spite of the different basic mechanisms behind resistance change and OTS occuring in a PCM cell, Ielmini *et al.* demonstrated a strong correlation between the resistance and threshold voltage of a partially SET/RESET cell.[61] In the I-V curves (fig. 4.11) of the cell states corresponding

to those characterized by R-I curves in fig. 4.10, the threshold voltage is evidently lower for a partially RESET/SET cell. In fact, they found a linear relationship between V_{Th} and R of the partially RESET/SET GST material after the resistance of the heater and selector had been factored out of the evaluations (fig. 4.12). Ielmini *et al.* argued that the linear correlation between V_{Th} with R implies a stacked or series configuration of amorphous and crystalline phases in the GST active volume of partically RESET/SET cell states. It has been known that threshold switching in amorphous chalcogenide alloys is driven by a critical electric field F_{crit}.[63] Hence, the V_{Th} of a cell depends linearly on the thickness of

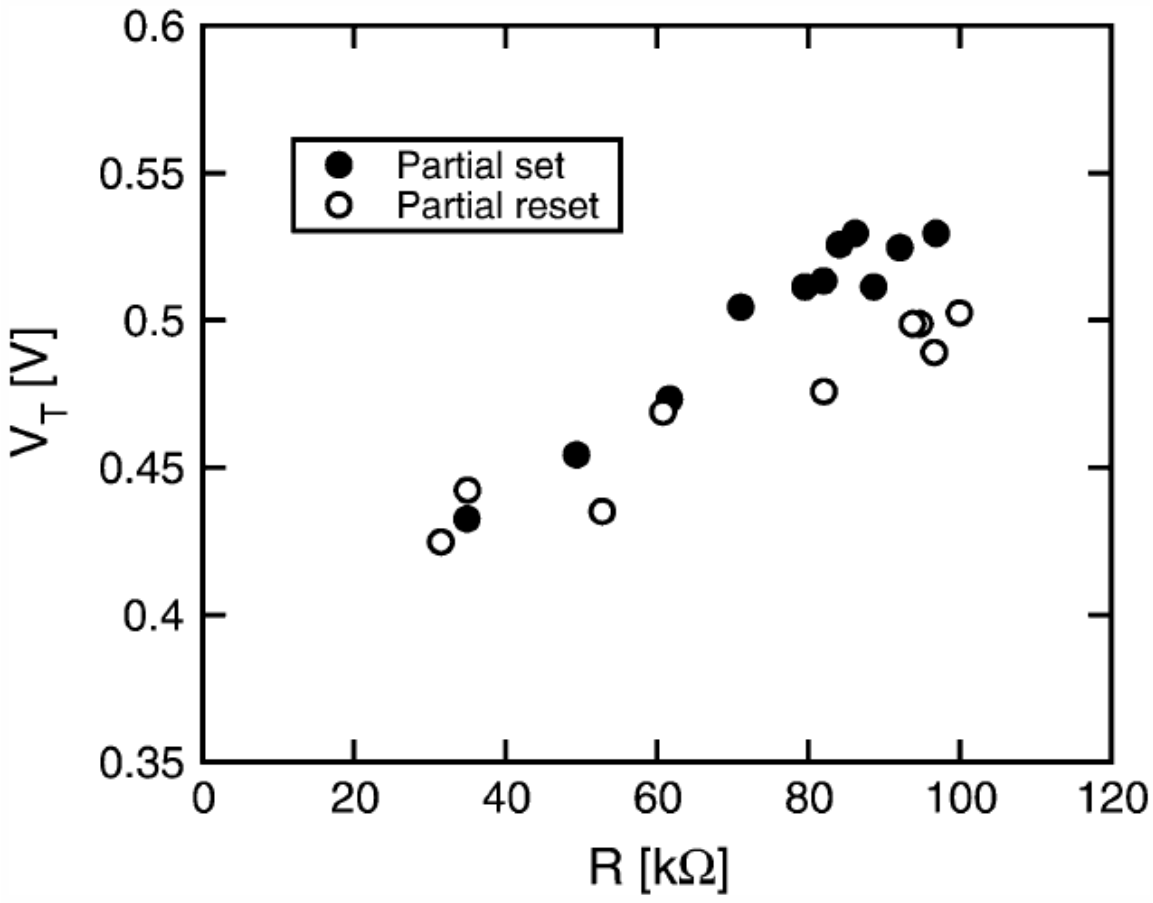


Figure 4.12: V_{Th} and Resistance correlation for partially RESET/SET cells.[61]

the amorphous GST thickness t_a as

$$V_{Th} = V_{Th0} + F_{crit} t_a \quad (4.1)$$

where V_{Th0} corresponds to the y-intercept of ~ 0.4 V in fig. 4.12, and is attributed to built-in potential drop at the contacts. The resistance R also scales linearly with amorphous fraction of the active volume as

$$R = \rho_a t_a / A_{eff} \quad (4.2)$$

where ρ_a is the resistivity of amorphous GST and A_{eff} is the effective cross-sectional area of the amorphous volume. From the above two equations, Ielmini *et al.* concluded that $V_{Th} - V_{Th0} \sim R$, reflecting the experimental data of fig. 4.12. They further pointed out that if the phase change and/or distribution in the active volume had been parallel, the correlation between V_{Th} and R as shown in Figure 4.12 would not be explicable by the two equations above, as the formation of the very first crystalline filament would limit the voltage across the cell to the "holding voltage" V_h (refer to fig. 4.7). This would in turn negate the gradual change in V_{Th} through partially RESET/SET states, as well as prevent OTS from occurring since the latter requires a potential drop of V_{Th} across the amorphous layer. Finally, they noted that the elements of phase change including nucleation, growth and melting being all temperature driven mechanisms, the boundaries of amorphous and crystalline phases should reflect the temperature profile during the programming pulse. Numerical simulations on the temperature profile during programming also indicate the likelihood of a stacked distribution of phases.

4.2 Improvement in PCM Cell Characteristics with Operational Cycles

In the backdrop of the preceding framework of knowledge, this dissertation chapter is based on developing an understanding for a phenomenon of gradual improvement in the figures of merit, viz. R_{SET}, R_{RESET}, and V_{Th}, with cycles of operation.

This improvement in the key figures of merit is observed to occur for ~ 10^4 normal cycles of operation of all typically well-functioning cells of a large, multi-megabit array without any evident degradation or breakdown, and is collectively referred to as "seasoning".

Figure 4.13 shows a cross-sectional TEM image of the active volume in amorphous and crystalline phases, where the dome-shaped amorphous region is clearly evident. In fig. 4.14 (a), the evolution of resistances of the two states as well as that of the threshold voltage with operational cycles is shown, where it must be noted that a cell in the virgin state (or, more accurately, after one cycle) already has sufficiently distinguishable memory states and is neither anomalous nor failing through the cycles. Thus, the cell is actually improved by the gradually widening memory window and increasing threshold voltage. The correlation between R_{Reset} and V_{Th} is also significantly evident through the cycles. Figure 4.14 (b) shows the R-I curves of a cell after 1 cycle and after it has undergone 10,000 cycles of operation. Apart from the improvement in the dynamic range (memory window) of the device after cycling, the RI curves also evidence a decreased requirement of programming current necessary to achieve a given resistance state of the cell, for both SET as well as RESET states. Conversely, a given programming

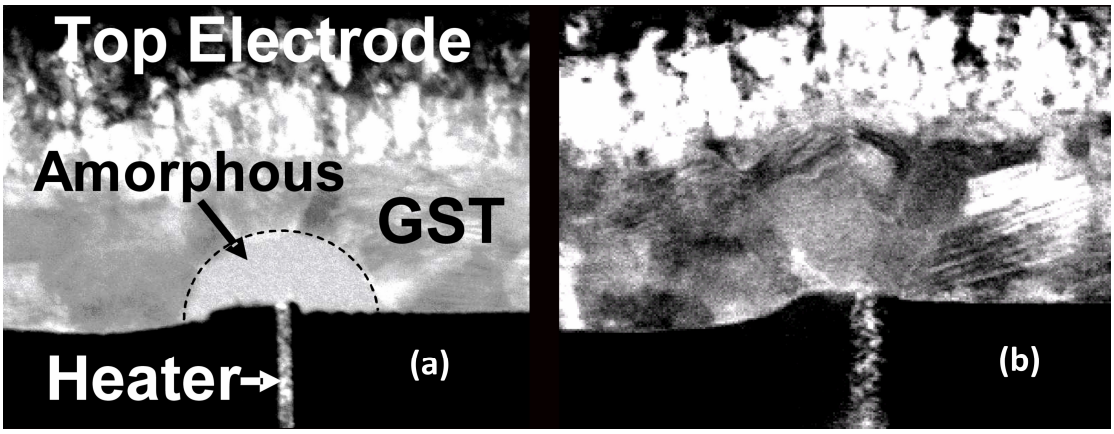
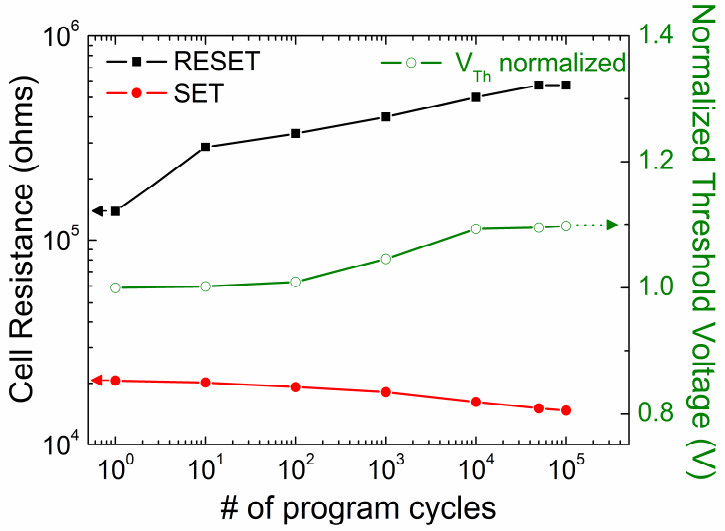
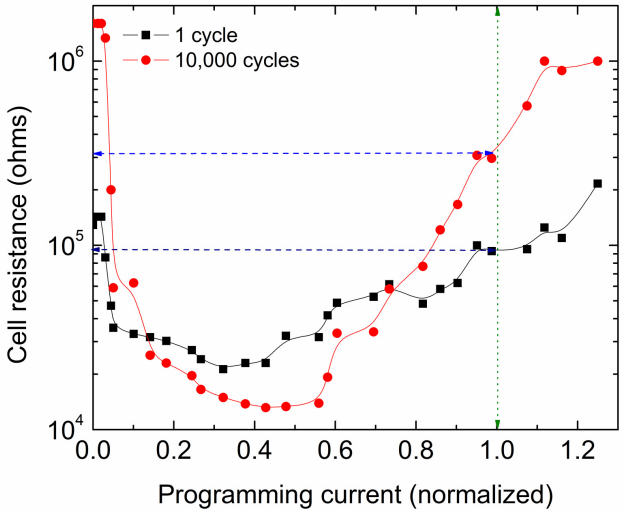


Figure 4.13: Cross-sectional Transmission Electron Micrographs showing (a) amorphous and (c) crystallized active volumes of GST.



(a)

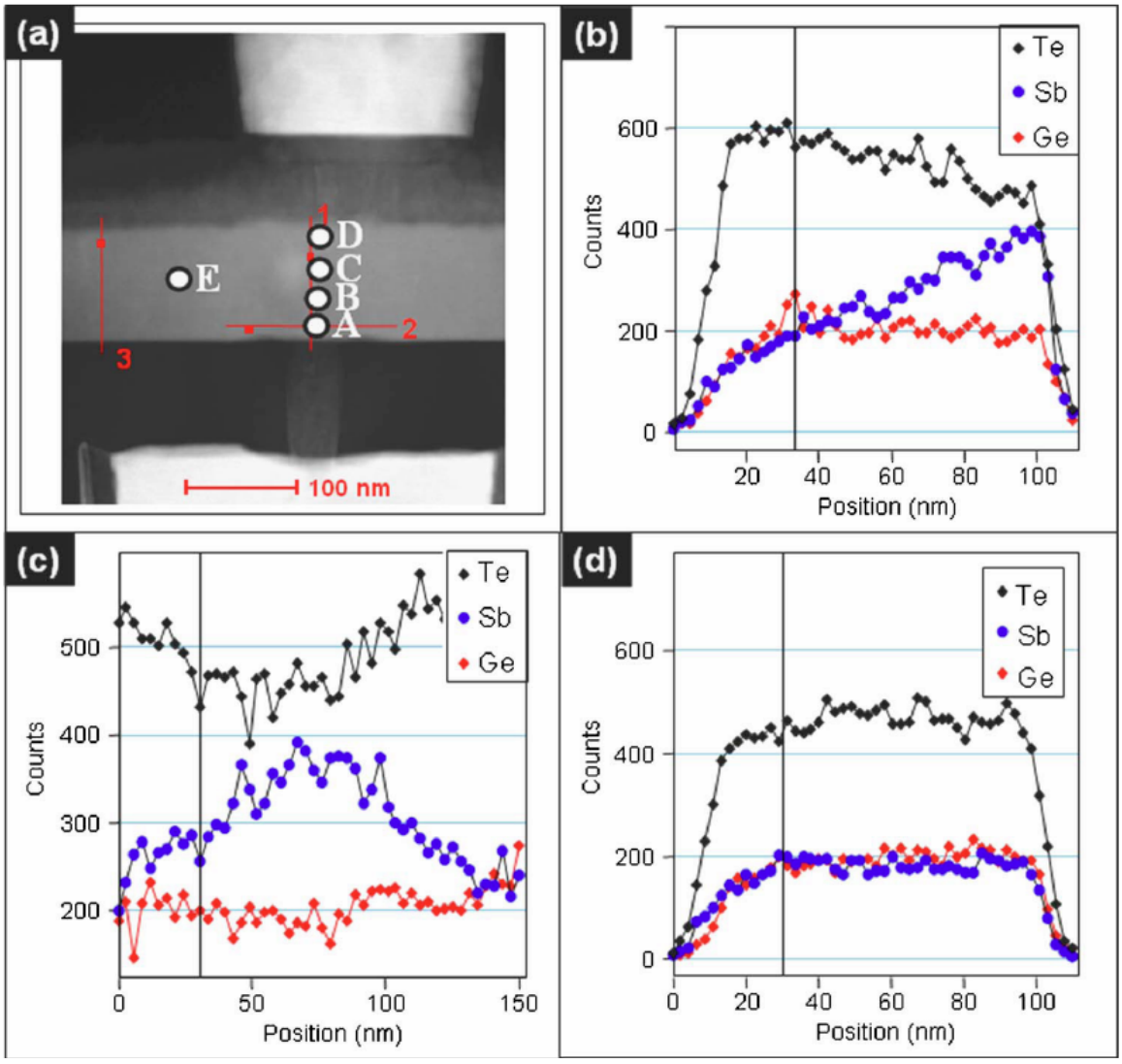


(b)

Figure 4.14: Characterization of seasoning showing (a) widening memory window and increasing threshold voltage for the median of a distribution of 25 kbits and, (b) RI curves of a cell showing a decreasing programming current requirement with operational cycles.

current is able to RESET (SET) the cell better by placing it to a higher (lower) RESET-state (SET-state) resistance, due to seasoning.

The fact that the change in cell electrical characteristics is a gradual, cumulative and permanent effect of RESET cycles indicates a gradual material transformation in the active volume of the GST layer. In this regard, recent material studies by Park *et al.* has provided direct evidence of compositional alteration of the pristine, stoichiometric $Ge_2T-e_2Sb_5$ in a very similar PCM cell, where the proportion of Te in the active volume (in crystalline as well as amorphous phases) is found to vary inversely with the temperature gradient during programming.[64] As shown in fig. 4.15, the proportion of Te (Sb) in the active volume GST is found to decrease (increase) in proportion to the increasing temperature profile across from the heater during programming. The Energy Dispersive Spectroscopy data clearly shows increasing Te (Sb) depletion (enrichment) at the points nearer to the heater (bottom electrode), while points far away from the heater show pristine stoichiometric $Ge_2Sb_2Te_5$ composition. Park *et al.* pointed out that the compositional variation of the GST qualitatively reflected the expected temperature profile based on simulations.[65] The localized Te-deficiency and accompanying Sb-enrichment is known to result from one or both of two causes. The first possible cause is a reaction between the heater Ti and the Te,[66] while the second is a segregation of Sb and Te within the GST layer due to the thermal stress associated with repeated melting.[67] Ryu *et al.* showed the compositional alteration of pristine $Ge_2Sb_2Te_5$ to $Ge_{15}Sb_{47}Te_{38}$ after programming of a PCM cell, and pointed out that the intrinsic high melting point of GST at 620 °C implied a likely inter-diffusion of the comprising elements between active and inactive GST regions during programming.[67] The electrical characterization studies undertaken as the subject of this chapter confirmed that melting (RESET operation) is



Element	A	B	C	D	E	*k*-factor
Ge(Kα)	21.78	21.08	20.37	22.60	23.03	1.000
Sb(Kα)	44.31	35.81	28.05	15.58	21.61	4.086
Te(Kα)	33.91	43.11	51.58	61.82	55.36	5.176

(e)

Figure 4.15: GST compositional analysis shows Te (Sb) depletion (enrichment) in proportion to the GST temperature during programming of PCM cell. (a) Scanning Transmission Electron Micrograph of PCM cell and, Energy Dispersive Spectrograph along lines (b) 1 (c) 2 and (d) 3. (e) GST %-compositions along points A – E shown in (a) [64]

necessary for seasoning to occur – programming without melting (SET or sub-threshold READ operations) is insufficient in producing any seasoning (data not shown). However, while Park *et al.* have reported observing the GST compositional change to occur unchanged irrespective of the number of RESET/SET cycles,[64] the electrical characterization data reported in fig. 4.14 is evidently a function of RESET cycles. This discrepancy could be due to any difference in the testing methodology and related difference in the defined virgin state of the investigated devices. As is apparent in fig. 4.14a, the most significant change in the R_{RESET} occurs between the first and the tenth programming cycle, underlining the criticality of the very first few electrical pulses on a fabricated device for seasoning.

Based on the electrical characterization data described herein, and material analysis reported by Ryu *et al.*, a physical model based on an evolving active volume of the GST with operational cycles is proposed in this chapter. A Te-deficient and Sb-rich non-stoichiometric GST (such as, $Ge_{15}Sb_{47}Te_{38}$) has been found to have a lower melting point ($\Delta \sim 70$ °C) and higher crystallization temperature ($\Delta \sim 40$ °C) compared to stoichiometric $Ge_2Sb_2Te_5$.[67] Further, the sheet resistance of $Ge_{15}Sb_{47}Te_{38}$ in crystalline state is about 100 times lower, while that in the amorphous state is similar or slightly lower than that of $Ge_2Sb_2Te_5$. Consequently, every cycle of melting of the GST with the associated compositional change is expected to lead to an increasing proportion of material in the active volume with a lower melting point, higher crystallization temperature and lower crystalline-state resistivity. However, since the energy input from the identical RESET pulse amplitude of every cycle remains unaltered, an increasingly larger volume of the compositionally-altered GST is expected to melt by virtue of its lower melting point. Therefore, every cycle of melting due to a RESET pulse would conceivably result in a gradual increase in the size of the active volume, as envisioned in

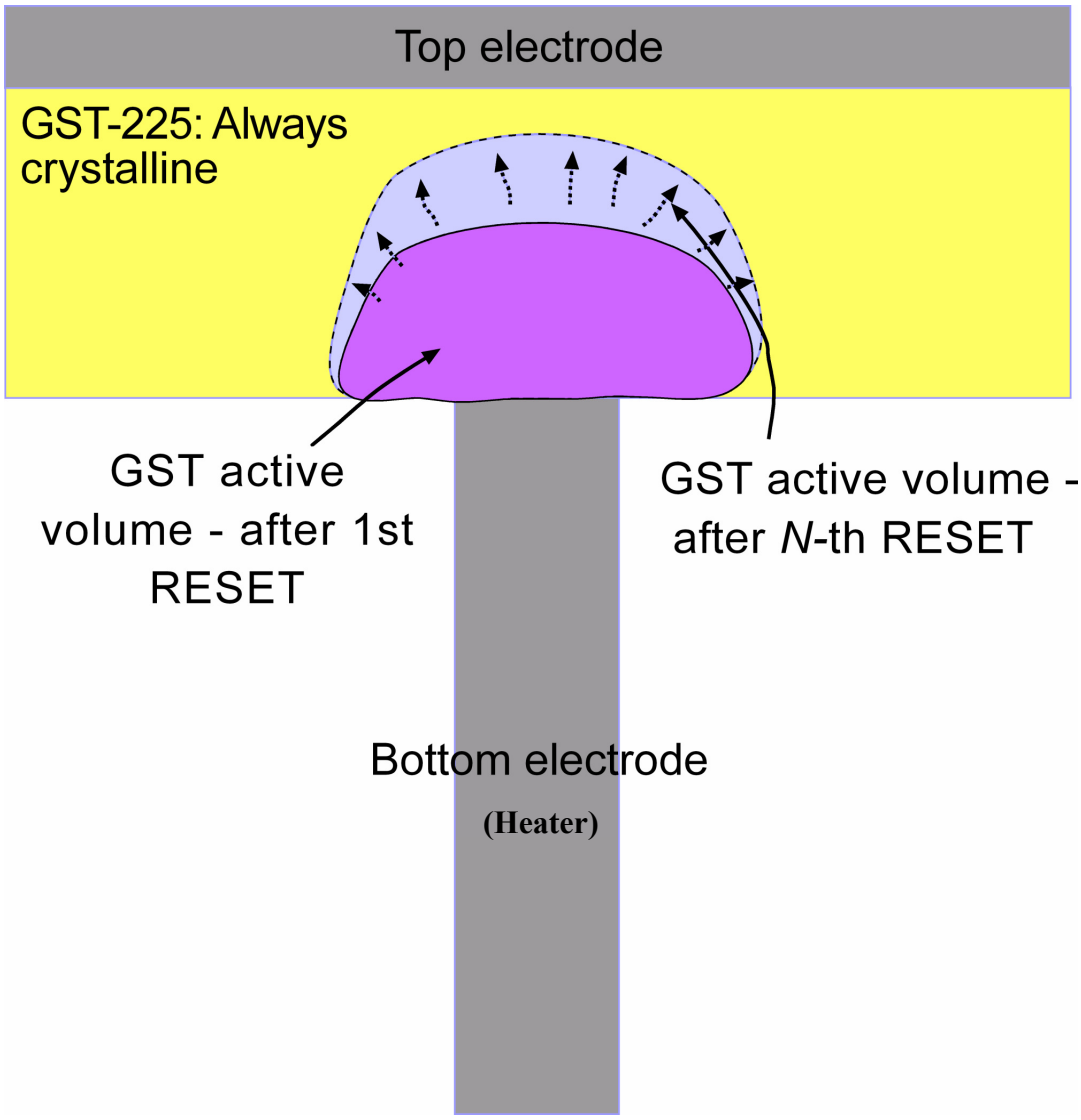


Figure 4.16: Proposed physical model involving an increasing volume of active material with operational cycles, to explain seasoning.

fig. 4.16. Since the resistance of a RESET cell is dependent on the size of the amorphous volume (eq. 4.2), the RESET-resistance increase with RESET-cycles is a direct consequence of this proposed model. On the other hand, the fact that the increasing active volume has significantly lower crystalline-phase resistivity than the *f.c.c*-phase of pristine

stoichiometric GST can explain the decreasing resistance of the SET-state with RESET cycles. Finally, V_{Th} being directly and linearly dependent on the amorphous GST thickness (eq. 4.1), an increasing V_{Th} with operational cycles is also a natural consequence of the proposed model.

While it is also possible that the interaction of the Ti of the heater (bottom electrode) with the Te in the GST is forming an interface layer that increases the cell resistance with cycles, the decrease in SET-state resistances and increase in V_{Th} imply that such an effect alone is not sufficient to explain seasoning. It may be noted that cross-sectional Transmission Electron Microscopy (TEM) on a cell can not be used to directly verify the model because of the inherently destructive nature of TEM. On the other hand, a comparison between the active volume of two different cells, one being cycled and another un-cycled may not be accurate or even observable because of process-induced variation between cells. Rigorous analytical and/or computational modeling based on the thermal and electrical ramifications of the compositional alteration in the three-dimensional active volume would be necessary to verify this proposed physical model. Based on the simplistic analytical dependence of the resistance-change (ΔR) with the increase in the radius (Δr) of a three-dimensional hemispherical active volume,

$$\Delta R \propto \frac{r_2 - r_1}{r_2 r_1} = \frac{\Delta r}{r_2 r_1} \tag{4.3}$$

an initial linear dependence followed by an asymptotic taper is expected (fig. 4.17), which is borne out in experimental data collected for cycle counts beyond 10^4 cycles (fig. 4.4a). It is also conceivable that an increasing active volume size would gradually lead to a thermal equilibrium with the top electrode, when increasing dissipation of heat would strongly contribute to arresting further increase in the active volume size.

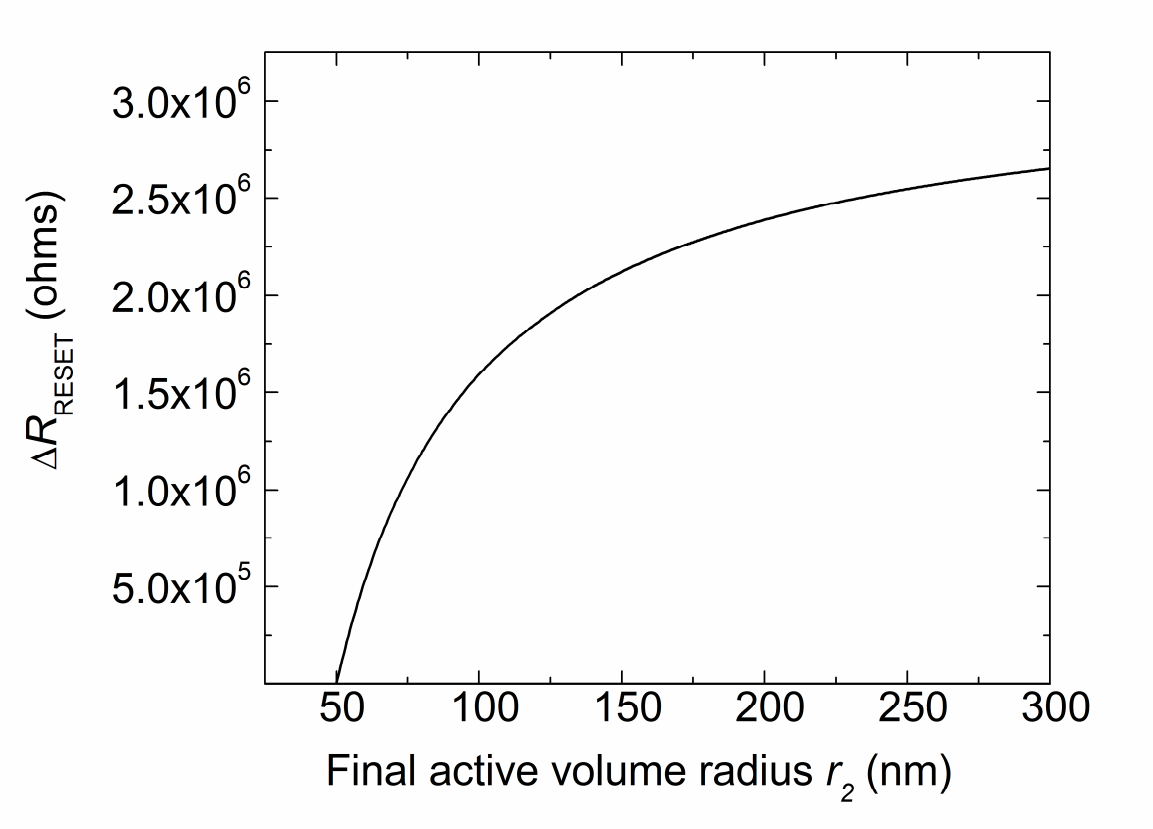


Figure 4.17: Plot of analytical dependence of RESET-state resistance increase with the increase in radius of three-dimensional hemispherical GST active volume (eq. 4.3). The resistance change is linear within ~ 100 % increase and, asymptotic beyond ~ 300 % increase in active volume radius (a bulk amorphous GST resistivity of 100 ohm-cm was used in the calculations)

A concern of slower SET switching speed has been cited against the compositional change of GST, attributable to the growth-dominated crystallization of Te-deficient GST as opposed to nucleation dominated crystallization of $Ge_2Sb_2Te_5$.[64] However, slower switching after 10,000 cycles was not observed within the limits of sub-microsecond SET pulse-widths tested in this study. It is known that the as-deposited GST in a PCM chip is in the stable hexagonal-close-packed (*h.c.p*) crystalline lattice after undergoing the thermal budget of backend processing (fig. 4.2b). On the other hand, the

re-crystallized SET-state of a non-virgin PCM cell has been shown to have GST active volume in the metastable face-centered-cubic (*f.c.c*) state.[64] The unchanged SET-speed in spite of the compositional transformation could be due to the active volume retaining the metastable *f.c.c* (or a hybrid) phase of GST through the operational cycles. Finally, the retention properties of the PCM cell would only be expected to improve from seasoning since the crystallization temperature and activation energy of Te-deficient GST is actually larger than that for $Ge_2Sb_2Te_5$.[67]

In summary, an improvement in the key figures of merit of a PCM cell with operational cycles was electrically characterized and correlated with recent reports of compositional alteration of the GST active volume. Based on the electrical characterization data and published material analysis, a physical model was proposed to self-consistently explain the observations, as an effort in developing fundamental understanding of PCM technology.

CHAPTER 5

Early and Erratic Data Retention Characterization of PCM Cells

For ascertaining the viability of a novel technology such as PCM replacing an entrenched technology such as Flash, careful analysis and understanding of all possible failure modes is necessary. In a large array product, statistical characterization of failing bits at the parts-per-million (PPM) level can reveal defect modes and mechanisms unforeseen at the level of individual cells. One such mechanism of early and erratic retention failure is characterized and discussed in this chapter for developing fundamental understanding of the reliability of nascent PCM technology.

5.1 Retention Characteristics of PCM Array and Cell

The memory retention characteristics of PCM is only fundamentally limited by the crystallization kinetics of the disordered, amorphous (RESET) state, since the ordered, crystalline state is the lowest energy state with very high activation energy. In other words, resistance loss of the amorphous phase of the memory material is the primary mode of information loss from a PCM cell. A statistical distribution for a large number of PCM cells comprising an array shows that the failure rate with temperature is well described by the Arrhenius equation and is distributed lognormally with time. The retention capability of typical cells exceeds 100,000 hours at 85 °C, thereby well

exceeding the requirement of 10 years at 85 °C for typical non-volatile memory applications.[68, 69] However, non-optimized devices have shown retention failures earlier than predicted by the lognormal distribution. The failure distribution of these non-optimized cells is Weibull with time but shows similar temperature acceleration as the intrinsic distribution, indicative of defect(s) in the amorphous chalcogenide material.

To characterize long retention time characteristics of PCM arrays, accelerated bake testing at elevated temperatures is used. The resistance of a RESET cell at elevated temperatures evolves with time as shown in fig. 5.1. Here, the cell was initially RESET to about 1 MΩ and the resistance is monitored at a constant 180 °C. The resistance of the cell initially increases due to "drift", which is a phenomenon characteristic of amorphous chalcogenides and caused by intrinsic trap dynamics.[70] Eventually, crystallization processes including nucleation, growth and finally, formation of a percolation path of crystallites across the amorphous volume leads to resistance loss of the cell.[71]

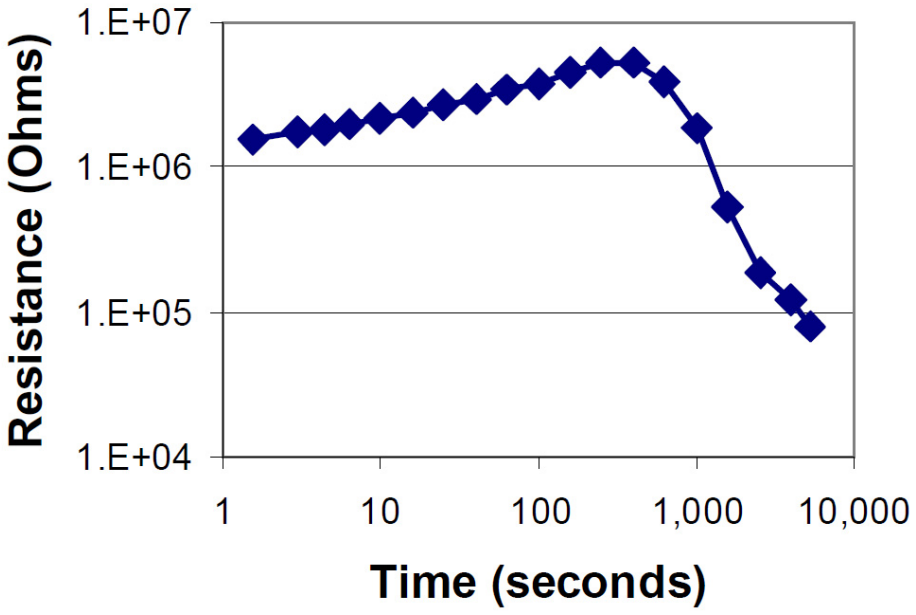


Figure 5.1: Resistance vs. time behavior of a typical RESET PCM cell at 180 °C.

At the array level, a similar behavior as shown in fig. 5.1 but with a broad distribution of data retention failure times is observed. For 512 kb of RESET cells undergoing successive high temperature bake steps for increasing time, a significant variation in crystallization time across the distribution of cells is found, as shown in fig 5.2. While the drift phenomenon is not clearly captured here due to the loss of measurement resolution above 1 MΩ, the cells were found to span between states that are fully SET (R < 10 kΩ) to fully RESET, after the completion of the final bake step.

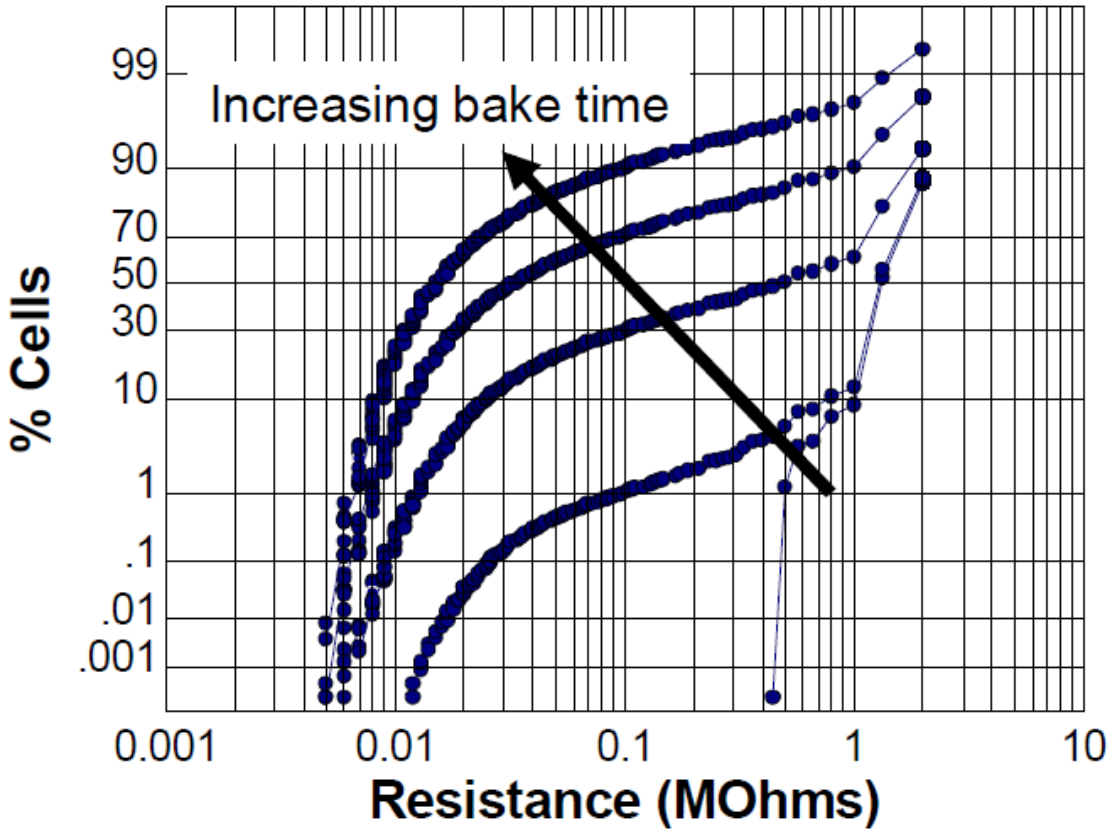


Figure 5.2: Resistance distribution variation of initially fully RESET 512 kb of PCM cells with increasing bake time at elevated temperature.

For estimating failure rates, an acceleration model for retention loss as a function of bake temperature was utilized. The experimental procedure comprised baking RESET arrays of cells at elevated temperatures until retention loss was observed, at which point the failure count was noted. The readouts were performed at room temperature and at a constant voltage of ~ 0.4 V. A cell resistance that dropped below 100 kΩ after a bake was counted as a retention failure. This procedure was then repeated at 160 °C, 140 °C and 125 °C on the same array cells and the failure count vs. accelerated bake time was then fit to the Arrhenius equation where time and temperature are related in the form:

$$t \propto \exp\left(\frac{E_a}{kT}\right)$$

With an activation energy E_a = 2.5 ± 0.1 eV, the simple Arrhenius model is able to describe the crystallization process within the range of temperatures under consideration, showing a lognormal distribution in time (fig. 5.3). The latter fact suggests that the retention failure at array level is driven by process variability as opposed to defect population. On scaling these data to 85 °C, a rather low memory retention failure rate less than 1 parts-per-billion at 100,000 hours is noted in fig. 5.3. Also, comparing the median time-to-failure for the array to single cell data collected between 180 °C and 210 °C,[72] shows an Arrhenius behavior across a wider range of temperatures as well, as shown in fig. 5.4

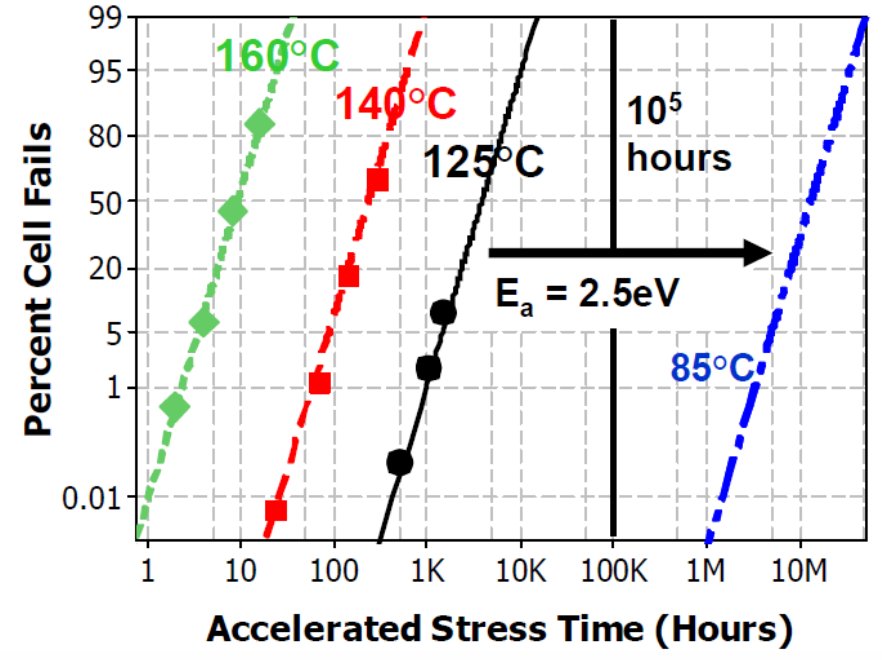


Figure 5.3: Data retention failure of PCM array cells as a function of time and temperature. The data are fit to an Arrhenius model with E_a = 2.5 eV and scaled to 85 °C.

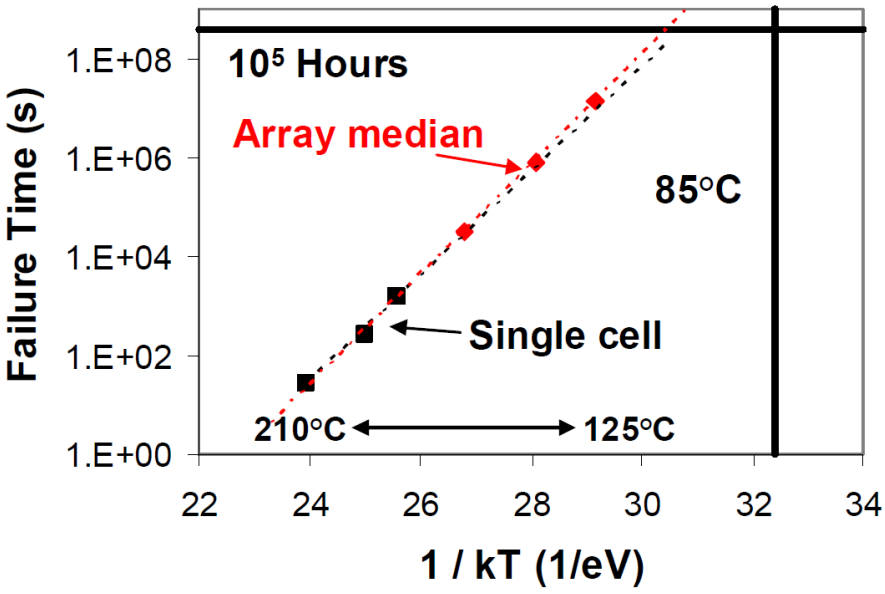


Figure 5.4: Arrhenius plot of data retention failure time vs. temperature, showing an overlap between single cell and array median data, for a wide range of temperatures.

5.2 Early and Erratic Retention Failures

The experimental methodology described above excluded studying cells that fail the very first accelerated bake test as due to extrinsic (process-induced) failures, and the involved failure mechanism for such initial failures may therefore be masked. Also, significant number of failing cells in the first readout at the elevated temperatures implies that an accurate estimation of time-to-failure of these initially failing cells remain uncertain. Therefore, assessing the risk of cells that do not fit the prior model and would fail earlier than the lognormal fit would predict must be considered.

Bake retention studies at lower temperatures than the previous experiments, specifically at 125 °C, 115 °C and 105 °C were performed to reveal early failing cells. These were best fit by a Weibull distribution consistent with a "defect" mechanism. The temperature dependence of these early failing cells however showed an $E_a = 2.4 \pm 0.1$ eV, suggesting that the crystallization process is not fundamentally altered between intrinsic and early failing cells.

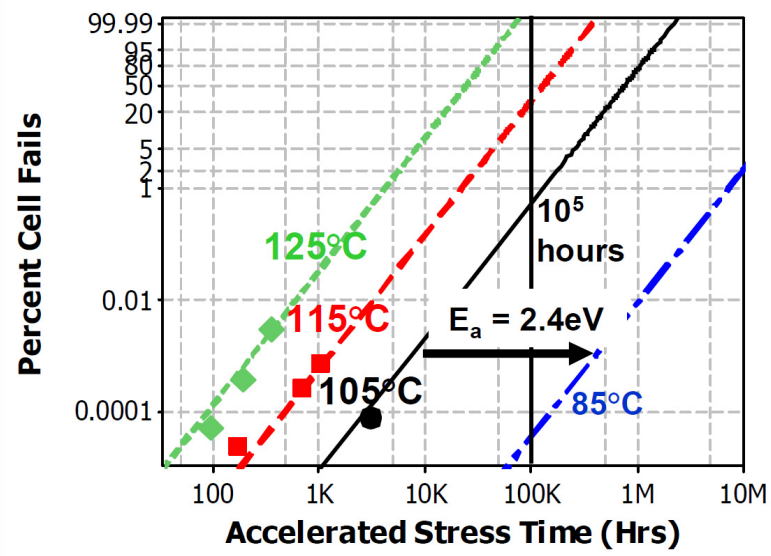


Figure 5.5: Early retention fail behavior as a function of bake time and temperature.

For developing an understanding of the early fail mechanism, a comparison between the initial (pre-bake) resistance of the erratic (early failed) cells with the intrinsic distribution is shown in fig. 5.6. While there is a bias for the erratic distribution towards a lower initial resistance, there is also a significant overlap with the intrinsic distribution, implying that the erratic cells are not clearly distinguishable from the intrinsic cells based on their initial resistance. This also indicates that the erratic cells are able to form an amorphous region that is electrically similar to the intrinsic (passing) cells.

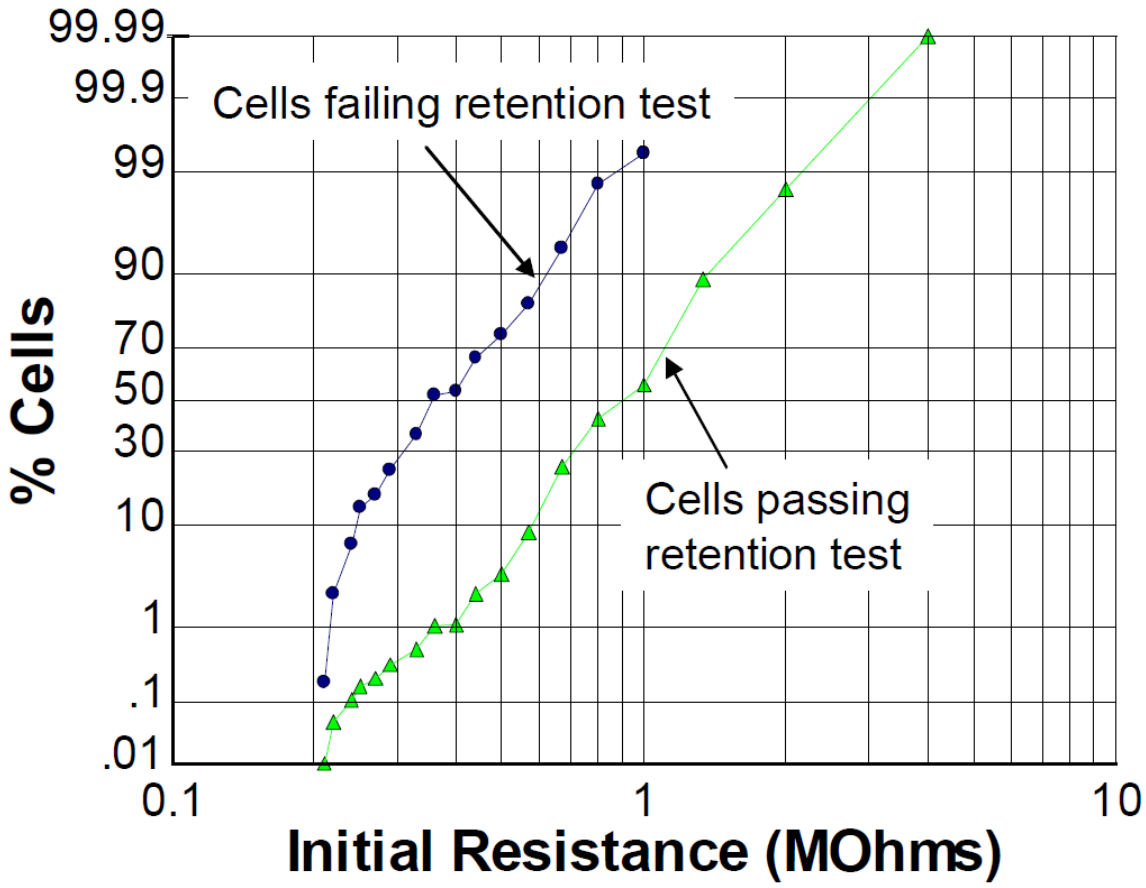


Figure 5.6: Initial resistance distribution comparison of cells with erratic (early failed) and intrinsic retention characteristics. The erratic cells failed a given retention test that the other (intrinsic) cells passed.

The fact that the erratic cells are similar to the intrinsic cells electrically, a deeper investigation of whether the failure mechanism is due to process-induced defects permanent to the cell or whether they were related to a weakness in the amorphous region dependent on the immediately prior RESET operation ("soft" defects) becomes necessary. The understanding developed there-in would determine if permanent defects could be eliminated via process improvement, modifications or screening methods at manufacturing, while soft defects would necessitate suppression of the failure mode via programming. Therefore, an experiment was devised where an array of cells were repeatedly RESET, baked and read for determining if the same set of cells failed through each bake. The first observation from this experiment was that the total number of failing cells was consistent through the repeated bake processes (to within 10 % accuracy). However, different individual cells had actually failed each time through the successive bakes, and only less than 1 % of cells failed repeatedly. Fig. 5.7 shows an example of this erratic retention failure going through multiple RESET-read-bake-read operations, where these representatively chosen set of specific cells failed the second bake test, but passed the first, third and fourth bake tests. This data indicates that the cells were all able to RESET very well prior to each of the bakes and consistently achieved the same RESET-state resistance every time they were written. Further, while all the cells failed the second bake (as they are selected by this criterion for representation in this plot), they also showed drift and modest resistance loss through the other bakes. This fact indicates that their erratic behavior in the second bake is unique to the particular RESET operation preceding the second bake, and any associated defect causing it must be associated with the nature and morphology of the amorphous volume resulting from that RESET operation. It also suggests a "bake-screen" at manufacturing would not be sufficient in removing such erratic failures in a large array of cells.

Figure 5.7: A representative behavior of erratic retention failed cells, where cells that failed Bake 2 passed the earlier and following bakes.

Based on the preceding data and analysis, mechanism of erratic retention seems to likely result not from a permanent defect in the cell, but from a unique property of the resulting amorphous active volume after any given RESET operations. The unchanged activation energy and high initial resistance of the erratic cells indicates that a small or otherwise deformed amorphous active volume is not the likely cause of the erratic behavior. Based on the crystallite growth model for retention loss, where pre-existing nucleation sites are arranged in a configuration such that very little growth is necessary

before resistance decrease is observed, a possible model was proposed by Gleixner *et al.* to explain the erratic retention behavior. For this model shown in fig. 5.8, it is assumed that nucleation sites exist in the amorphous active volume of all cells after every RESET operation; and resistance decrease is caused by the growth of these nuclei to join and form a percolation path across the amorphous active volume. With every RESET operation, a different configuration of these nucleation sites would result, and if the average number of nuclei is fairly constant over the entire population of cells, this model can explain the erratic retention failure for cells based on the unlikely alignment of the nucleation sites leading to an early or erratic failure. It is worth noting that a programming optimization as well as a process modification was also reported by Gleixner *et al.* as successful schemes suppressing the erratic retention failures.[73]

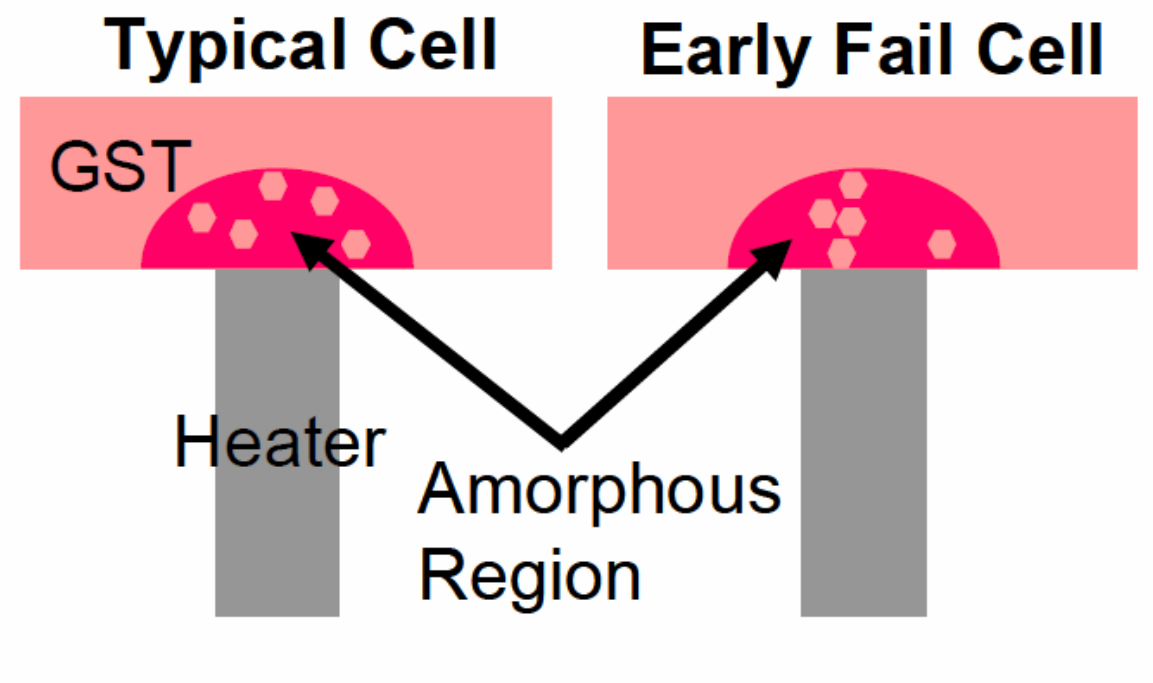


Figure 5.8: Schematic representation of a model for failure of the early or erratic cell, based on a configuration of pre-existing nuclei in the amorphous active volume resulting from the preceding RESET pulse, which can lead to faster resistance loss than that for a typical cell.[73]

In summary, single cell and array data retention characteristics was studied and understanding was developed for the early and erratic retention failure modes of PCM technology. While the intrinsic retention characteristics of PCM technology appears robust and sufficient for exceeding requirements of typical non-volatile memory applications, non-intrinsic failure modes specific to PCM technology must be dealt with for a large, dense array product. To this end, understanding was developed for mitigation of such a retention failure mode in nascent PCM technology.

CHAPTER 6

Conclusion

6.1 Summary and Conclusion

Non-volatile memory physics and technology is at a critical and interesting juncture of its evolution where the conventional, planar Flash transistor has nearly exhausted its scaling potential. Therefore, the future improvements in density, performance and cost-per-bit would likely involve a re-thinking of the cell architecture and/or a switch to an alternate technology. The integration of nanocrystal floating-gate with the vertical transistor can possibly infuse long-term scaling possibilities into traditional charge-based non-volatile memory technology while leveraging decades of research and developmental work on the metal-oxide-semiconductor physics and technology. On the other hand, a radical switch-over to an alternate non-volatile memory technology with long-term scaling potential, such as Phase Change Memory that can also leverage the research and development on chalcogenide material used in CD/DVD media, is another promising path-way. The leading semiconductor non-volatile memory manufacturers have wagered on either of the two approaches with significant research and development budget, indicating that a move to non-conventional planar Flash or alternative material-based technologies is imminent in the near future. The research work described in this dissertation aims to further those efforts with a hope for contributing to the march of technology in enhancing and improving our society.

6.2 Suggested Future Work

The most obvious future research work in the realm of the vertical Flash transistor with nanocrystal floating-gate would be incorporation of high-K dielectrics in the gate-stack for low-power and/or greater speed. The future implementation of high-K dielectrics in logic technology announced by the dominant industry players such as Intel and IBM bodes well for investigations on incorporating the same for non-volatile memory, especially considering the more limited scaling potential of the Flash transistor compared to the logic transistor. Ultimately, the vertical transistor architecture can also lend itself well for bottom-up growth methods of producing nanowire and carbon-nanotube based devices. Thus, the potential of the traditional metal-oxide semiconductor based devices would likely be realized to the fullest by exploring both traditional and self-assembled three-dimensional transistors along with few-electron physics of nanocrystal charge storage.

As already mentioned, significant understanding of phase-change memory technology has been achieved in the last few years for its production as a mainstream non-volatile technology in the next few years. The avenues of research in PCM technology are many, especially considering the scaling potential and expectations of the nascent technology. Thermal disturbs, techniques for programming current reduction, material degradation and material integration are challenges to be overcome for successful evolution and scalability of the technology for the next decade. On the other hand, since the evolution of PCM technology is not nearly as fundamentally limited by the laws of physics as is the planar Flash transistor, the future of phase change technology appears promising.

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Vita

Joy Sarkar was born to Bharati and Tapan Kumar Sarkar on October 26th, 1977 at Kanpur, India. The only child of his parents, Joy attended Don Bosco School, Liluah, and Calcutta Boys School from kindergarten to high school. He earned the Bachelor of Science (Hons.) degree in Physics from the Indian Institute of Technology, Kharagpur in 2000. In 2001 he joined Rice University on a Dean's Fellowship and was later appointed a research assistant to Prof. Alex Rimberg, who supervised his thesis for the Master of Science degree in Applied Physics titled "Engineering the Electromagnetic Environment of a Nanostructure to Study Single-electron Tunneling". After graduating from Rice in 2004, he joined the University of Texas at Austin for the Doctor of Philosophy degree in Electrical and Computer Engineering (Solid-State Electronics) supervised by and as a research assistant to Prof. Sanjay K. Banerjee. He interned with Intel Corporation working in the Phase Change Memory team at Folsom (Summer, 2005) and at Santa Clara (Summer 2006 and Spring-Fall 2007), California, which culminated in his dissertation being co-supervised by his manager Dr. Robert J. Gleixner. After graduating with the PhD degree, he expects to continue with Intel Corporation as a Senior Reliability Engineer in the Phase Change Memory Quality and Reliability group.

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